LCM-TFT050T1

产品名称（**Product name**）：彩色 **TFT** 模组

型　　号（**Model**）：LCM-TFT050T1SVP16R40D

编　　号（**Part number**）：20200418

日　　期（**Date**）：2020-4-18

深圳市鑫洪泰电子科技有限公司 **Shenzhen Hot Display Technology Co.,Ltd**		
编制	审核	核准

Rev.	Descriptions	Date
01	Prelimiay Release	2020-4-18

Table of Content

5 Inch TFT Display Module LCM-TFT050T1

Product characteristics

1， Contains SSD1963, TP driver(XPT2046), booster circuit。
2， Backlight brightness can be adjusted by PWM from SSD1963。
3， Interface width can be selected: 8/16 bits。
4， Can realize part of a display vertical scrolling。
5， Order of the columns and pages can be selected。
6， Order of the RGB can be selected。
7， Display color depth can be selected。

1. Basic Specifications

1.1 Drive Specifications

1>LCD Display Mode	a-SI,TFT, 5.0',Transmissive
2>Viewing Angle	Full view
3>Driving Method	Graphic 800（R+G+B）x 480 Dots-matrix
4>Interface	8080 MPU parallel interface(8/16 Bits Bus)
5>Backlight:	12 Pcs White LED
6>Controller/Driver	SSD1963

1.2 Mechanical Specifications

1>Outline Dimension	143.5(L)x81 (W)x8.2(H)mm(Detailed Information refer to LCM Drawing)
2>Active Area	108(L)x64.8(W)
3>Pixel Pitch	0.153(L)x0.153(W)

1.3 Absolute Maximum Ratings

Items	Symbol	MIN.	MAX.	Unit	Condition
Power Supply Voltage	Vcc	-0.3	5.5	V	-
Input Voltage	VIN	-0.3	3.5	V	-
LCD Driver Supply Voltage	VGH-VSS	-0.3	18.5	V	-
Operating Temperature	TOP	-20	+70	℃	-
Storage Temperature	Tst	-30	+85	℃	-
Storage Humidity	Hd	-	Ta<40	℃	-

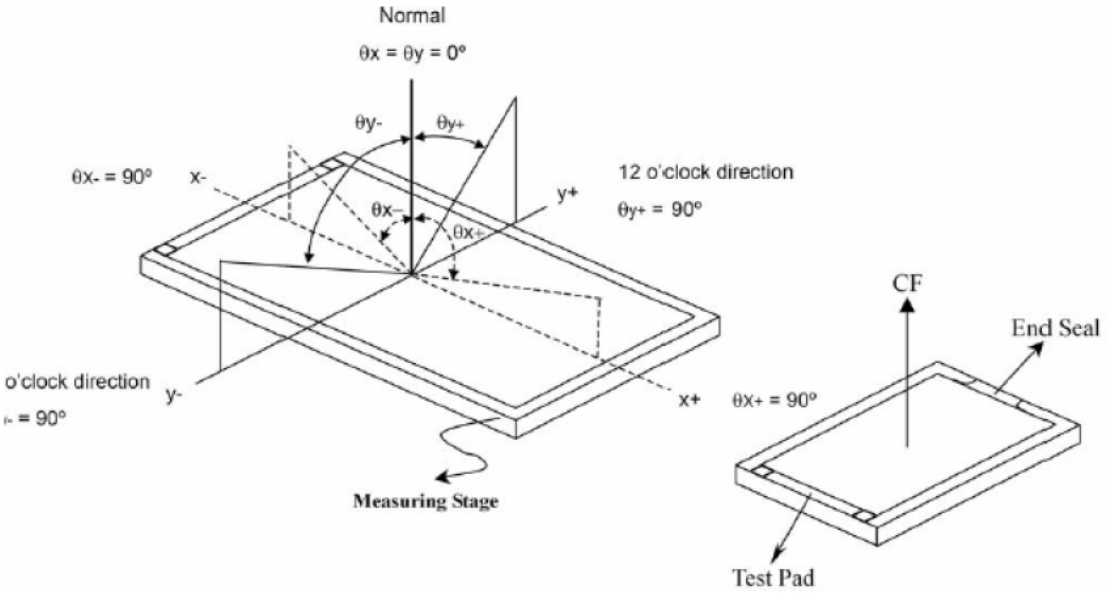
1.4 DC Electrical Characteristics

Items	Symb	MIN.	TYP.	MAX.	Unit	Condition
Logic Supplay	IOVC	2.7	3.3	3.6	V	-
Input High Voltage	VIH	0.8 IOVCC	--	IOVCC	V	-
Input Low Voltage	VIL	-0.3	-	0.2 IOVCC	V	-
Output H Voltage	VOH	0.8 IOVCC		IOVCC	V	-
Output L Voltage	VOL	-0.3	-	0.2 IOVCC	V	-
Supply Current	I	-	40	-	mA	VCC=3.3V

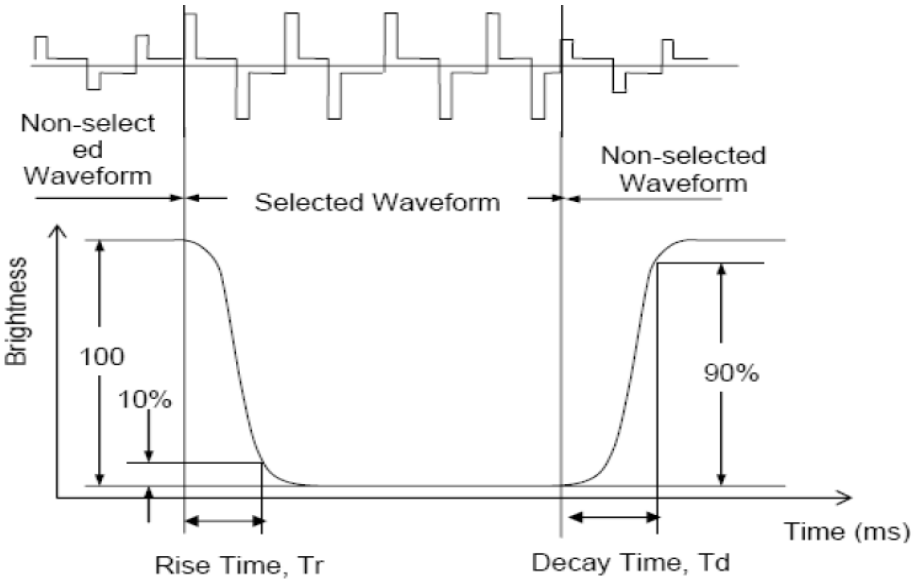
1.5 Optical Characteristics

Items	Symbol		MIN.	TYP.	MAX.	Reference	Condition
View Angle	Hor	θ L	-	85	-	Note5-1	CRε 10 B / L on
		θ R	-	85	-	Note5-1	
	Ver	Φ H	-	85	-	Note5-1	
		Φ L	-	85	-	Note5-1	
Contrast Ratio	C		-	300	-	-	θ =0° , Φ=0
Response	tr		-	TBD	-	Note5-2	θ =0° , Φ=0
Response Time(fall)	tf		-	TBD	-	Note5-2	θ =0° , Φ=0
Luminance	B		200	450		Cd/m^2	θ =0° , ϕ =0

Note 5-1 The definitions of viewing angles:



Note 5-2 Response time is defined as follow



1.6 Backlight & LED Characteristics

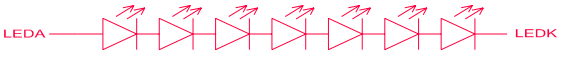
Maximum Ratings

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Forword Voltage	V_F	–	19. 6	–	V	I_F = 40mA
Forword Current	IF	-	40	-	mA	PWM=255
Power Dissipation	P_{WF}		800	-	mW	W=20V*40mA

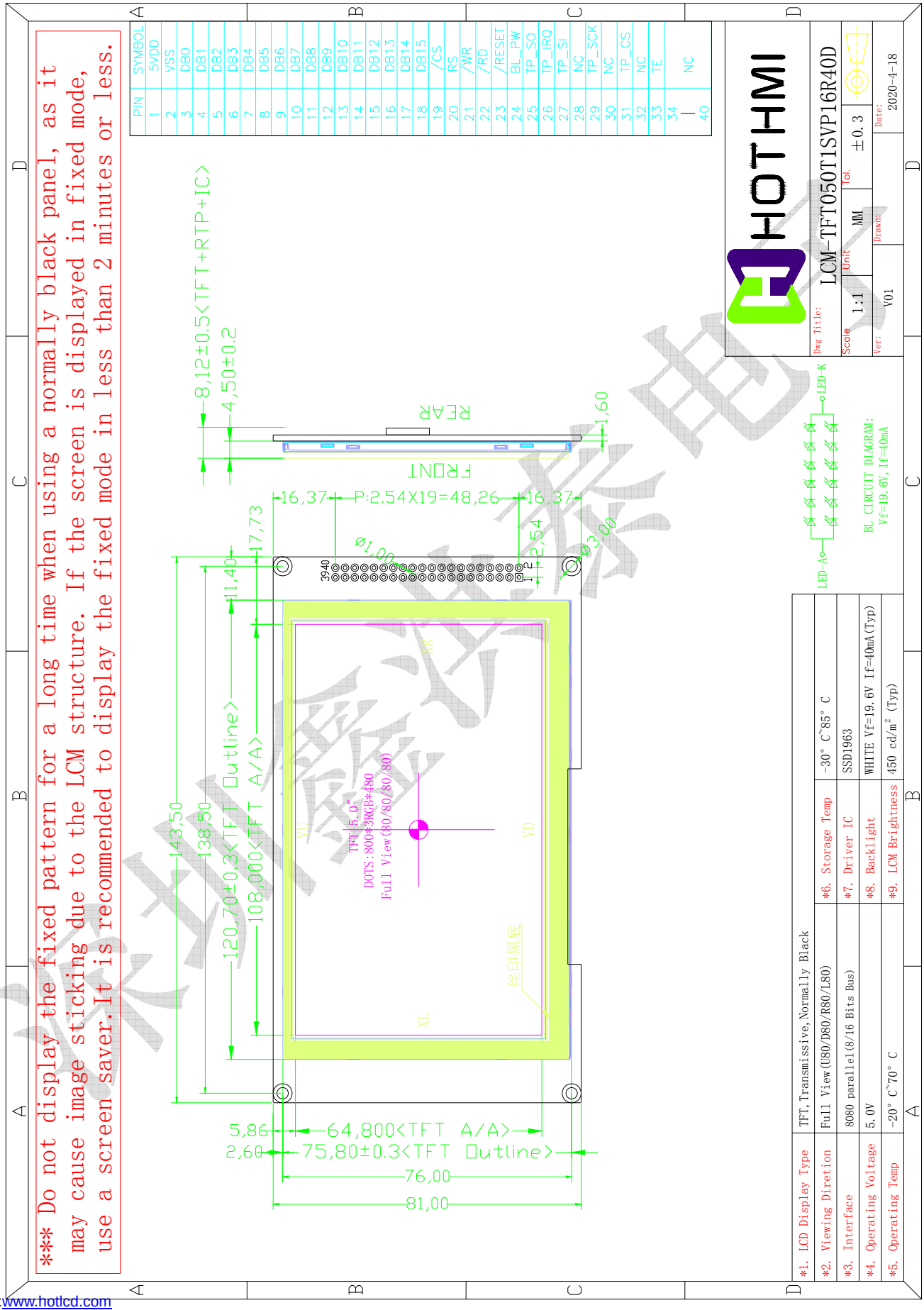
Electrical/Optical Characteristics **VSS=0V,Ta=25℃**

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Forword Voltage	VF	-	19.6	-	V	IF=40Ma
Reverse Current	IR	-	-	10	uA	VR=10V
Average Brightness (without LCD)	IV	2800	5000	-	cd/m^2	IF=15mA
CIE Color Coordinate (without LCD)	X	0.26	-	0.300	-	IF=15mA
	Y	0.26	-	0.300		
Color	WHITE					

***1 Thie value will be change while mass production.**



2. Structure Block


*** Do not display the fixed pattern for a long time when using a normally black panel, as it may cause image sticking due to the LCM structure. If the screen is displayed in fixed mode, use a screen saver. It is recommended to display the fixed mode in less than 2 minutes or less.
PIN SYMBOL
1 5VDD
2 VSS
3 DB0
4 DB1
5 DB2
6 DB3
7 DB4
8 DB5
9 DB6
10 DB7
11 DB8
12 DB9
13 DB10
14 DB11
15 DB12
16 DB13
17 DB14
18 DB15
19 /CS
20 RS
21 /WR
22 /RD
23 /RESET
24 BL_PW
25 TP_SO
26 TP_IRQ
27 TP_SI
28 NC
29 TP_SCK
30 NC
31 TP_CS
32 NC
33 TE
34 — NC
40
HOTHMI
Dwg Title: LCM-TFT050T1SVP16R40D
Scale 1:1
Unit MM
Tol. ±0.3
Drawn:
Ver: V01
Date: 2020-4-18
8,12±0.5<TFT+RTP+IC>
4,50±0.2
REAR
FRONT
1,60
16,37
P:2.54X19=48,26
16,37
17,73
11,40
2,54
3,00
Ø1,00
3940
143,50
138,50
120,70±0.3<TFT Outline>
108,000<TFT A/A>
TFT 5.0"
DOTS:800*3(RGB)*480
Full View(80/80/80/80)
XR
XL
YU
YD
丝印黑底
5,86
2,60
64,800<TFT A/A>
75,80±0.3<TFT Outline>
76,00
81,00
LED-K
LED-A
BL CIRCUIT DIAGRAM:
Vf=19.6V, If=40mA
*1. LCD Display Type TFT, Transmissive, Normally Black
*2. Viewing Direction Full View(U80/D80/R80/L80)
*3. Interface 8080 parallel(8/16 Bits Bus)
*4. Operating Voltage 5.0V
*5. Operating Temp -20°C~70°C
*6. Storage Temp -30°C~85°C
*7. Driver IC SSD1963
*8. Backlight WHITE Vf=19.6V If=40mA(Typ)
*9. LCM Brightness 450 cd/m² (Typ)

3 Terminal Function

Pin No.	Pin Name	I/O	Function
1	VDD	P	Power Supply (5V)
2	GND	P	Ground (0V)
3	DB0-DB15	I/O	16-Bit parallel interface
|			
18			
19	/CS	I	Chip Select Signal /CS = L, enable Access To The LCD module
20	RS	I	Data Type Select RS=L, Command Write, RS=H, Data Write
21	/WR	I	Write Enable Input
22	/RD	I	Read Enable Input
23	/RESET	I	/RESET = H, Normal Running /RESET = L, Initialization is executed
24	BL_EN	I	
25	RTP_SO	O	Serial Data Output. Data is shifted on the falling
26	RTP_IRQ	O	Pen Interrupt.
27	RTP_SI	I	Serial Data Input. If CS is LOW, data is latched on
28	-		
29	RTP_SCK	I	External Clock Input to RTP
30	-		
31	RTP_CS	I	Chip Select Input
32	-		
33	TE	O	Tearing effect
34	-		
|			
40			

4. Interface specifications

TBD

5 Command Table

Hex Code	Command	Description
0x 00	nop	No operation
0x 01	soft_reset	Software Reset
0x 0A	get_power_mode	Get the current power mode
0x 0B	get_address_mode	Get the frame memory to the display panel read order
0x 0C	get_pixel_format	Get the current pixel format
0x 0D	get_display_mode	The display module returns the Display Signal Mode.
0x 0E	get_signal_mode	Get the current display mode from the peripheral
0x 0F	Reserved	Reserved
0x 10	enter_sleep_mode	Turn off the panel. This command will pull low the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x 11	exit_sleep_mode	Turn on the panel. This command will pull high the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x 12	enter_partial_mode	Part of the display area is used for image display.
0x 13	enter_normal_mode	The whole display area is used for image display.
0x 20	exit_invert_mode	Displayed image colors are not inverted.
0x 21	enter_invert_mode	Displayed image colors are inverted.
0x 26	set_gamma_curve	Selects the gamma curve used by the display device.
0x 28	set_display_off	Blanks the display device
0x 29	set_display_on	Show the image on the display device
0x 2A	set_column_address	Set the column extent
0x 2B	set_page_address	Set the page extent
0x 2C	write_memory_start	Transfer image information from the host processor interface to the peripheral starting at the location provided by set_column_address and set_page_address
0x 2E	read_memory_start	Transfer image data from the peripheral to the host processor interface starting at the location provided by set_column_address and set_page_address
0x 30	set_partial_area	Defines the partial display area on the display device
0x 33	set_scroll_area	Defines the vertical scrolling and fixed area on display area
0x 34	set_tear_off	Synchronization information is not sent from the display module to the host processor
0x 35	set_tear_on	Synchronization information is sent from the display module to the host processor at the start of VFP
0x 36	set_address_mode	Set the read order from frame buffer to the display panel
0x 37	set_scroll_start	Defines the vertical scrolling starting point
0x 38	exit_idle_mode	Full color depth is used for the display panel
0x 39	enter_idle_mode	Reduce color depth is used on the display panel.
0x 3A	set_pixel_format	Defines how many bits per pixel are used in the interface
0x 3C	write_memory_continue	Transfer image information from the host processor interface to the peripheral from the last written location
0x 3E	read_memory_continue	Read image data from the peripheral continuing after the last read_memory_continue or read_memory_start
0x 44	set_tear_scanline	Synchronization information is sent from the display module to the host processor when the display device refresh reaches the provided scanline

Hex Code	Command	Description
0x 45	get_scanline	Get the current scan line
0x A1	read_ddb	Read the DDB from the provided location
0x A8	Reserved	Reserved
0x B0	set_lcd_mode_	Set the LCD panel mode (RGB TFT or TTL)
0x B1	get_lcd_mode	Get the current LCD panel mode, pad strength and resolution
0x B4	set_hori_period	Set front porch
0x B5	get_hori_period	Get current front porch settings
0x B6	set_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0x B7	get_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0x B8	set_gpio_conf	Set the GPIO configuration. If the GPIO is not used for LCD, set the direction. Otherwise, they are toggled with LCD signals.
0x B9	get_gpio_conf	Get the current GPIO configuration
0x BA	set_gpio_value	Set GPIO value for GPIO configured as output
0x BB	get_gpio_status	Read current GPIO status. If the individual GPIO was configured as input, the value is the status of the corresponding pin. Otherwise, it is the programmed value.
0x BC	set_post_proc	Set the image post processor
0x BD	get_post_proc	Set the image post processor
0x BE	set_pwm_conf	Set the image post processor
0x BF	get_pwm_conf	Set the image post processor
0x C0	set_lcd_gen0	Set the rise, fall, period and toggling properties of LCD signal generator 0
0x C1	get_lcd_gen0	Get the current settings of LCD signal generator 0
0x C2	set_lcd_gen1	Set the rise, fall, period and toggling properties of LCD signal generator 1
0x C3	get_lcd_gen1	Get the current settings of LCD signal generator 1
0x C4	set_lcd_gen2	Set the rise, fall, period and toggling properties of LCD signal generator 2
0x C5	get_lcd_gen2	Get the current settings of LCD signal generator 2
0x C6	set_lcd_gen3	Set the rise, fall, period and toggling properties of LCD signal generator 3
0x C7	get_lcd_gen3	Get the current settings of LCD signal generator 3
0x C8	set_gpio0_rop	Set the GPIO0 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO0 is configured as general GPIO.
0x C9	get_gpio0_rop	Get the GPIO0 properties with respect to the LCD signal generators.
0x CA	set_gpio1_rop	Set the GPIO1 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO1 is configured as general GPIO.
0x CB	get_gpio1_rop	Get the GPIO1 properties with respect to the LCD signal generators.
0x CC	set_gpio2_rop	Set the GPIO2 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO2 is configured as general GPIO.
0x CD	get_gpio2_rop	Get the GPIO2 properties with respect to the LCD signal generators.

Hex Code	Command	Description
0x CE	set_gpio3_rop	Set the GPIO3 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO3 is configured as general GPIO.
0x CF	get_gpio3_rop	Get the GPIO3 properties with respect to the LCD signal generators.
0x D0	set_dbc_conf	Set the dynamic back light configuration
0x D1	get_dbc_conf	Get the current dynamic back light configuration
0x D4	set_dbc_th	Set the threshold for each level of power saving
0x D5	get_dbc_th	Get the threshold for each level of power saving
0x E0	set_pll	Start the PLL. Before the start, the system was operated with the crystal oscillator or clock input
0x E2	set_pll_mn	Set the PLL
0x E3	get_pll_mn	Get the PLL settings
0x E4	get_pll_status	Get the current PLL status
0x E5	set_deep_sleep	Set deep sleep mode
0x E6	set_lshift_freq	Set the LSHIFT (pixel clock) frequency
0x E7	get_lshift_freq	Get current LSHIFT (pixel clock) frequency setting
0x E8	Reserved	Reserved
0x E9	Reserved	Reserved
0x F0	set_pixel_data_interface	Set the pixel data format of the parallel host processor interface
0x F1	get_pixel_data_interface	Get the current pixel data format settings
0x FF	Reserved	Reserved

6 Command Descriptions

6.1 Software Reset

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	0	0	0	0	1	01

The display module performs a software reset. Only the configuration register will be reset.

6.2 Enter Sleep Mode

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	1	0	0	0	0	10

Turn off the panel.This command causes the display panel to enter sleep mode and pull low the GPIO0.
If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command Set GPIO Conf(0xB8), this command will not affect the GPIO0.

6.3 Enter Partial Mode

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	1	0	0	1	0	12

6.4 Enter Normal Mode

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	1	0	0	1	1	13

6.5 Enter Normal Mode

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	1	0	0	1	1	13

This command causes the display module to stop inverting the image data on the display device. The frame buffer contents remain unchanged

6.6 Enter Invert Mode

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	0	0	0	0	1	21

This command causes the display module to invert the image data only on the display device.The frame buffer contents remain unchanged.

6.7 Set Gamma Curve

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	0	0	1	1	0	26
Parameter 1	1	0	0	0	0	A_3	A_2	A_1	A_0	xx

Selects the gamma curve used by the display device.

A[3:0]	Gamma curve selection (POR = 1000)	GAMAS[1]	GAMAS[0]
0000	No gamma curve selected (Same as 0001b)	0	0
0001	Gamma curve 0	0	0
0010	Gamma curve 1	0	1
0100	Gamma curve 2	1	0
1000	Gamma curve 3	1	1
Others	Reserved		

6.8 Set Display On/Off

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	0	1	0	0	S	28/29

If S=1, Show the image on the display device;
If S=0, Blanks the display device. The frame buffer contents remain unchanged.

6.9 Set Column Address

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	0	1	0	1	0	2A
Parameter 1	1	SC_{15}	SC_{14}	SC_{13}	SC_{12}	SC_{11}	SC_{10}	SC_9	SC_8	xx
Parameter 2	1	SC_7	SC_6	SC_5	SC_4	SC_3	SC_2	SC_1	SC_0	xx
Parameter 3	1	EC_{15}	EC_{14}	EC_{13}	EC_{12}	EC_{11}	EC_{10}	EC_9	EC_8	xx
Parameter 4	1	EC_7	EC_6	EC_5	EC_4	EC_3	EC_2	EC_1	EC_0	xx

Set the column extent of frame buffer accessed by the host processor with the Read Me mory Continue, 0x3E and Write Memory Continue, 0x3C
SC[15:8] : Start column number high byte (POR = 00000000)
SC[7:0] : Start column number low byte (POR = 00000000)
EC[15:8] : End column number high byte (POR = 00000000)
EC[7:0] : End column number low byte (POR = 00000000)

6.10 Set Page Address

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	0	1	0	0	1	2B
Parameter 1	1	SP_{15}	SP_{14}	SP_{13}	SP_{12}	SP_{11}	SP_{10}	SP_9	SP_8	xx
Parameter 2	1	SP_7	SP_6	SP_5	SP_4	SP_3	SP_2	SP_1	SP_0	xx
Parameter 3	1	EP_{15}	EP_{14}	EP_{13}	EP_{12}	EP_{11}	EP_{10}	EP_9	EP_8	xx
Parameter 4	1	EP_7	EP_6	EP_5	EP_4	EP_3	EP_2	EP_1	EP_0	xx

Set the page extent of the frame buffer accessed by the host processor with the Read M emory Co ntinue, 0x3E and Write
Memory Continue, 0x3C.
SP[15:8] : Start page (row) number high byte (POR = 00000000)
SP[7:0] : Start page (row) number low byte (POR = 00000000)
EP[15:8] : End page (row) number high byte (POR = 00000000)

EP[7:0] : End page (row) number low byte (POR = 00000000)

6.11 Write Memory Start

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	0	1	1	0	0	2C

Transfer image information from the host processor interface to the SSD1963 starting at the location provided by Set Column Address, 0x2A and Set Page Address, 0x2B.

6.12 Read Memory Start

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	0	1	1	1	0	2E

Transfer image data from the SSD1963 to the host processor interface starting at the location provided by Set Column Address, 0x2A and Set Page Address, 0x2B.

6.13 Set Partial Area

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	0	0	0	0	30
Parameter 1	1	SR_{15}	SR_{14}	SR_{13}	SR_{12}	SR_{11}	SR_{10}	SR_9	SR_8	xx
Parameter 2	1	SR_7	SR_6	SR_5	SR_4	SR_3	SR_2	SR_1	SR_0	xx
Parameter 3	1	ER_{15}	ER_{14}	ER_{13}	ER_{12}	ER_{11}	ER_{10}	ER_9	ER_8	xx
Parameter 4	1	ER_7	ER_6	ER_5	ER_4	ER_3	ER_2	ER_1	ER_0	xx

This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER). SR and ER refer to the Frame Buffer Line Pointer.
SR[15:8] : Start display row number high byte (POR = 00000000)
SR[7:0] : Start display row number low byte (POR = 00000000)
ER[15:8] : End display row number high byte (POR = 00000000)
ER[7:0] : End display row number low byte (POR = 00000000)
Note : SR[15:0] and ER[15:0] cannot be 0000h nor exceed the last vertical line number.

6.14 Set Scroll Area

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	0	0	1	1	33
Parameter 1	1	TFA_{15}	TFA_{14}	TFA_{13}	TFA_{12}	TFA_{11}	TFA_{10}	TFA_9	TFA_8	xx
Parameter 2	1	TFA_7	TFA_6	TFA_5	TFA_4	TFA_3	TFA_2	TFA_1	TFA_0	xx
Parameter 3	1	VSA_{15}	VSA_{14}	VSA_{13}	VSA_{12}	VSA_{11}	VSA_{10}	VSA_9	VSA_8	xx
Parameter 4	1	VSA_7	VSA_6	VSA_5	VSA_4	VSA_3	VSA_2	VSA_1	VSA_0	xx
Parameter 5	1	BFA_{15}	BFA_{14}	BFA_{13}	BFA_{12}	BFA_{11}	BFA_{10}	BFA_9	BFA_8	xx
Parameter 6	1	BFA_7	BFA_6	BFA_5	BFA_4	BFA_3	BFA_2	BFA_1	BFA_0	xx

Defines the vertical scrolling and fixed area on display area
TFA[15:8] : High byte of Top Fixed Area number in lines from the top of the frame buffer (POR = 00000000) TFA[7:0] : Low byte of Top Fixed Area number in lines from the top of the frame buffer (POR = 00000000)
VSA[15:8] : High byte of Vertical scrolling area in number of lines of the frame buffer (POR =

00000000) VSA[7:0] : Low byte of Vertical scrolling area in number of lines of the frame buffer (POR = 00000000)

BFA[15:8] : High byte of Bottom Fixed Area in number of lines from the bottom of the frame buffer (POR = 00000000) BFA[7:0] : Low byte of Bottom Fixed Area in number of lines from the bottom of the frame buffer (POR = 00000000)

6.15 Set Tear Off

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	0	1	0	0	34

TE signal is not sent from the display module to the host processor.

6.16 Set Tear On

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	0	1	0	1	35
Parameter 1	1	0	0	0	0	0	0	0	A_0	xx

TE signal is sent from the display module to the host processor at the start of VFP.

A[0] : Tearing effect line mode (POR = 0)

0 The tearing effect output line consists of V-blanking information only.

1 The tearing effect output line consists of both V-blanking and H-blanking information.

The TE signal shall be active low when the display panel is in Sleep mode.

6.17 Set Address Mode

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	0	1	1	0	36
Parameter 1	1	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	xx

Set the read order from host processor to frame buffer by A[7:5] and A[3] and from frame buffer to the display panel by A[2:0] and A[4].

A[7] : Page address order (POR = 0)

This bit controls the order that pages of data are transferred from the host processor to the SSD1963's frame buffer.

0 Top to bottom, pages transferred from SP (Start Page) to EP (End Page).

1 Bottom to top, pages transferred from EP (End Page) to SP (Start Page).

A[6] : Column address order (POR = 0)

This bit controls the order that columns of data are transferred from the host processor to the SSD1963's frame buffer.

0 Left to right, columns transferred from SC (Start Column) to EC (End Column).

1 Right to left, columns transferred from EC (End Column) to SC (Start Column).

A[5] : Page / Column order (POR = 0)

This bit controls the order that columns of data are transferred from the host processor to the SSD1963's frame buffer.

0 Normal mode

1 Reverse mode

A[4] : Line address order (POR = 0)

This bit controls the display panel's horizontal line refres h order. The image shown on the display panel is unaffected, regardless of the bit setting.

0 LCD refresh from top line to bottom line.

1 LCD refresh from bottom line to top line.

A[3] : RGB / BGR order (POR = 0)

This bit controls the RGB data order transferred from the SSD1963's frame buffer to the display panel.

0 RGB

1 BGR

A[2] : Display data latch data (POR = 0)

This bit controls the display panel's vertical line data latch order. The image shown on the display panel is unaffected, regardless of the bit setting.

0 LCD refresh from left side to right side

1 LCD refresh from right side to left side

A[1] : Flip Horizontal (POR = 0)

This bit flips the image shown on the display panel left to right. No change is made to the frame memory.

0 Normal

1 Flipped

A[0] : Flip Vertical (POR = 0)

This bit flips the image shown on the display panel top to bottom. No change is made to the frame memory.

0 Normal

1 Flipped

6.18 Set Scroll Start

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	0	1	1	1	37
Parameter 1	1	VSP_{15}	VSP_{14}	VSP_{13}	VSP_{12}	VSP_{11}	VSP_{10}	VSP_9	VSP_8	xx
Parameter 2	1	VSP_7	VSP_6	VSP_5	VSP_4	VSP_3	VSP_2	VSP_1	VSP_0	xx

This command sets the start of the vertical scrolling area in the frame buffer. The vertical scrolling area is fully defined when this command is used with the Set Scroll Area 0x33.

VSP[15:8] : High byte of Vertical Scroll Pointer to define the line number in frame buffer that is written to the display as the first line of the vertical scrolling area (POR = 00000000)

VSP[7:0] : Low byte of Vertical Scroll Pointer to define the line number in frame buffer that is written to the display as the first line of the vertical scrolling area (POR = 00000000)

6.19 Exit Idle Mode

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	1	0	0	S	38/39

If S=0, This command causes the display module to exit Idle Mode. Full color depth is used for the display panel.

If S=1, This command causes the display module to enter Idle Mode.

In Idle Mode, color depth is reduced. Colors are shown on the display panel using the MSB of each of the R, G and B color components in the frame buffer.

6.20 Set Pixel Format

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	1	0	1	0	3A
Parameter 1	1	0	A_6	A_5	A_4	0	0	0	0	xx

Set the current pixel format for RGB image data

A[6:4] : Display pixel format (POR = 000)

000 Reserved
001 3-bit/pixel
010 8-bit/pixel
011 12-bit/pixel
100 Reserved
101 16-bit/pixel
110 18-bit/pixel
111 24-bit/pixel

6.21 Write Memory Continue

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	1	1	0	0	3C

Transfer image information from the host processor interface to the SSD1963 from the last Write Memory Continue, 0x3C or Write Memory Start, 0x2C.

6.22 Read Memory Continue

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	1	1	1	1	1	0	3E

Read image data from the SSD1963 to host processor continuing after the last Read Memory Continue, 0x3E or Read Memory Start, 0x2E.

6.23 Set LCD Mode

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	0	1	1	0	0	0	0	B0
Parameter 1	1	0	0	A_5	A_4	A_3	A_2	A_1	A_0	xx
Parameter 2	1	B_7	B_6	B_5	0	0	0	0	0	xx
Parameter 3	1	0	0	0	0	0	HPS_{10}	HPS_9	HPS_8	xx
Parameter 4	1	HPS_7	HPS_6	HPS_5	HPS_4	HPS_3	HPS_2	HPS_1	HPS_0	xx
Parameter 5	1	0	0	0	0	0	VPS_{10}	VPS_9	VPS_8	xx
Parameter 6	1	VPS_7	VPS_6	VPS_5	VPS_4	VPS_3	VPS_2	VPS_1	VPS_0	xx
Parameter 7	1	0	0	G_5	G_4	G_3	G_2	G_1	G_0	xx

Set the LCD panel mode (RGB TFT or TTL) and pad strength

A[5] : TFT panel data width (POR = 0)

0 18-bit
1 24-bit

A[4] : TFT color depth enhancement enable (POR = 0)

0 Disable FRC or dithering
1 Enable FRC or dithering for color depth enhancement

If the panel data width was set to 24-bit, FRC and dithering feature will be disabled automatic

regardless the value of this register.

A[3] : TFT FRC enable (POR = 0)
0 TFT dithering enable
1 TFT FRC enable

A[2] : LSHIFT polarity (POR = 0)
Set the dot clock pulse polarity.
0 Data latch in rising edge
1 Data latch in falling edge

A[1] : LLINE polarity (POR = 0)
Set the horizontal sync pulse polarity.
0 Active low
1 Active high

A[0] : LFRAME polarity (POR = 0)
Set the vertical sync pulse polarity.
0 Active low
1 Active high

B[7] : LCD panel mode (POR = 0)
0 Hsync+Vsync +DE mode
1 TTL mode

B[6:5] : TFT type (POR = 01)
00, 01 TFT mode
10 Serial RGB mode
11 Serial RGB+dummy mode

HPS[10:8] : Set the horizontal panel size (POR = 010)
HPS[7:0] : Set the horizontal panel size (POR = 01111111)
Horizontal panel size = (HPS + 1) pixels

VPS[10:8] : Set the vertical panel size (POR = 001)
VPS[7:0] : Set the vertical panel size (POR = 11011111)
Vertical panel size = (VPS + 1) lines

G[5:3] : Even line RGB sequence (POR = 000)
000 RGB
001 RBG
010 GRB
011 GBR
100 BRG

101 BGR
11x Reserved

G[2:1] : Odd line RGB sequence (POR = 000)
000 RGB
001 RBG
010 GRB
011 GBR
100 BRG
101 BGR
11x Reserved

6.24 Set Horizontal Period

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	0	1	1	0	1	0	0	B4
Parameter 1	1	0	0	0	0	0	HT_{10}	HT_9	HT_8	xx
Parameter 2	1	HT_7	HT_6	HT_5	HT_4	HT_3	HT_2	HT_1	HT_0	xx
Parameter 3	1	0	0	0	0	0	HPS_{10}	HPS_9	HPS_8	xx
Parameter 4	1	HPS_7	HPS_6	HPS_5	HPS_4	HPS_3	HPS_2	HPS_1	HPS_0	xx
Parameter 5	1	0	HPW_6	HPW_5	HPW_4	HPW_3	HPW_2	HPW_1	HPW_0	xx
Parameter 6	1	0	0	0	0	0	LPS_{10}	LPS_9	LPS_8	xx
Parameter 7	1	LPS_7	LPS_6	LPS_5	LPS_4	LPS_3	LPS_2	LPS_1	LPS_0	xx
Parameter 8	1	0	0	0	0	0	0	$LPSPP_1$	$LPSPP_0$	xx

Set front porch

HT[10:8] : High byte of horizontal total period (display + non-display) in pixel clock (POR = 010)
HT[7:0] :
Low byte of the horizontal total period (display + non-display) in pixel clock (POR = 10101111)
Horizontal total period = (HT + 1) pixels

HPS[10:8] : High byte of the non-display period between the start of the horizontal sync (LLINE) signal and the first display data. (POR = 000)
HPS[7:0] : Low byte of the non-display period between the start of the horizontal sync (LLINE) signal and the first display data. (POR = 00100000)

For TFT : Horizontal Sync Pulse Start Position = (HPS + 1) pixels
For Serial TFT : Horizontal Sync Pulse Start Position = (HPS + 1) pixels + LPSPP subpixels
HPW[6:0] : Set the horizontal sync pulse width (LLINE) in pixel clock. (POR = 000111)
Horizontal Sync Pulse Width = (HPW + 1) pixels

LPS[10:8] : Set the horizontal sync pulse (LLINE) start location in pixel clock. (POR = 000)
LPS[7:0] : Set the horizontal sync pulse width (LLINE) in start. (POR = 00000000)
Horizontal Display Period Start Position = LPS pixels

LPSPP[1:0] : Set the horizontal sync pulse subpixel start position (POR = 00)

6.25 Set Vertical Period

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	0	1	1	0	1	1	0	B6
Parameter 1	1	0	0	0	0	0	VT_{10}	VT_9	VT_8	xx
Parameter 2	1	VT_7	VT_6	VT_5	VT_4	VT_3	VT_2	VT_1	VT_0	xx
Parameter 3	1	0	0	0	0	0	VPS_{10}	VPS_9	VPS_8	xx
Parameter 4	1	VPS_7	VPS_6	VPS_5	VPS_4	VPS_3	VPS_2	VPS_1	VPS_0	xx
Parameter 5	1	0	VPW_6	VPW_5	VPW_4	VPW_3	VPW_2	VPW_1	VPW_0	xx
Parameter 6	1	0	0	0	0	0	FPS_{10}	FPS_9	FPS_8	xx
Parameter 7	1	FPS_7	FPS_6	FPS_5	FPS_4	FPS_3	FPS_2	FPS_1	FPS_0	xx

Set the vertical blanking interval between last scan line and next LFRAME pulse

VT[10:8] : High byte of the vertical total (display + non-display) period in lines (POR = 001)
VT[7:0] : Low byte of the vertical total (display + non-display) period in lines (POR = 11101111)
Vertical Total = (VT + 1) lines

VPS[10:8] : High byte the non-display period in lines between the start of the frame and the first display data in line. (POR = 000)
VPS[7:0] : The non-display period in lines between the start of the frame and the first display data in line. (POR = 00000100)
Vertical Sync Pulse Start Position = VPS lines

VPW[6:0] : Set the vertical sync pulse width (LFRAME) in lines. (POR = 000001)
Vertical Sync Pulse Width = (VPW + 1) lines

FPS[10:8] : High byte of the vertical sync pulse (LFRAME) start location in lines. (POR = 000)
FPS[7:0] : Low byte of the vertical sync pulse (LFRAME) start location in lines. (POR = 00000000)
Vertical Display Period Start Position = FPS lines

6.26 Set Post Proc

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	0	1	1	1	1	0	0	BC
Parameter 1	1	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	xx
Parameter 2	1	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	xx
Parameter 3	1	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	xx
Parameter 4	1	0	0	0	0	0	0	0	D_0	xx

Set the image post processor

A[7:0] : Set the contrast value (POR = 01000000)

B[7:0] : Set the brightness value (POR = 10000000)

C[7:0] : Set the saturation value (POR = 01000000)

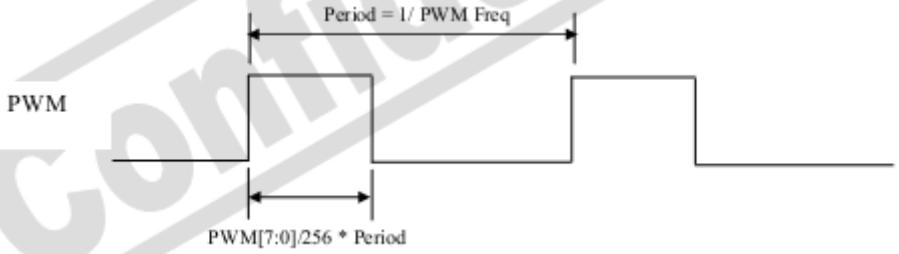
D[0] : Post Processor Enable (POR = 0)
0 Disable the postprocessor
1 Enable the postprocessor

6.27 Set PWM Configuration

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	0	1	1	1	1	1	0	BE
Parameter 1	1	$PWMF_7$	$PWMF_6$	$PWMF_5$	$PWMF_4$	$PWMF_3$	$PWMF_2$	$PWMF_1$	$PWMF_0$	xx
Parameter 2	1	PWM_7	PWM_6	PWM_5	PWM_4	PWM_3	PWM_2	PWM_1	PWM_0	xx
Parameter 3	1	0	0	0	0	C_3	0	0	C_0	xx
Parameter 4	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	xx
Parameter 5	1	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0	xx
Parameter 6	1	0	0	0	0	F_3	F_2	F_1	F_0	xx

Set the PWM configuration
PWMF[7:0] : Set the PWM frequency in system clock (POR = 00000000)
PWM signal frequency = PLL clock / (256 * PWMF[7:0]) / 256

PWM[7:0] : Set the PWM duty cycle (POR = 00000000)
PWM duty cycle = PWM[7:0] / 256
Note : PWM always 0 if PWM[7:0] = 00h



C[3] : PWM configuration (POR = 0)
0 PWM controlled by host
1 PWM controlled by DBC

C[0] : PWM enable (POR = 0)
0 PWM disable
1 PWM enable

D[7:0] : DBC manual brightness (POR = 00000000)
Set the brightness level
00 Dimmest
FF brightest

E[7:0] : DBC minimum brightness (POR = 00000000)
Set the minimum brightness level
00 Dimmest
FF Brightest
F[3:0] : Brightness prescaler (POR = 0000)
Set the brightness prescaler
0 Dimmest
F Brightest

6.28 Set LCD Gen0

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	0	0	0	0	0	0	C0
Parameter 1	1	A_7	0	0	0	0	0	0	0	xx
Parameter 2	1	0	0	0	0	0	$GF0_2$	$GF0_1$	$GF0_0$	xx
Parameter 3	1	$GF0_7$	$GF0_6$	$GF0_5$	$GF0_4$	$GF0_3$	$GF0_2$	$GF0_1$	$GF0_0$	xx
Parameter 4	1	0	0	0	0	0	$GR0_2$	$GR0_1$	$GR0_0$	xx
Parameter 5	1	$GR0_7$	$GR0_6$	$GR0_5$	$GR0_4$	$GR0_3$	$GR0_2$	$GR0_1$	$GR0_0$	xx
Parameter 6	1	F_7	F_6	F_5	F_4	F_3	$GP0_2$	$GP0_1$	$GP0_0$	xx
Parameter 7	1	$GP0_7$	$GP0_6$	$GP0_5$	$GP0_4$	$GP0_3$	$GP0_2$	$GP0_1$	$GP0_0$	xx

Set the rise, fall, period and toggling properties of LCD signal generator 0

A[7] : Reset LCD generator 0 at every frame start
- 0 The generator 0 will not reset in the starting point of a frame
- 1 The generator 0 will reset in the starting point of a frame

GF0[10:8] : The highest 3 bits of the generator 0 falling position (POR = 000)
GF0[7:0] : The lower byte of the generator 0 falling position (POR = 00000001)

GR0[10:8] : The highest 3 bits of the generator 0 rising position (POR = 000)
GR0[7:0] : The lower byte of the generator 0 rising position (POR = 00000000)

F[7] : Force the generator 0 output to 0 in non-display period
- 0 generator 0 is normal
- 1 generator 0 output is forced to zero in non-display period

F[6:5] : Force the generator 0 output to 0 in odd or even lines
- 00 generator 0 is normal in both odd and even lines
- 01 generator 0 output is force to 0 in odd lines
- 10 generator 0 output is force to 0 in even lines
- 11 generator 0 is normal in both odd and even line

F[4:3] : Generator 0 toggle mode
- 00 Disable
- 01 Toggle by pixel clock (LSHIFT)
- 10 Toggle by Line (LLINE)
- 11 Toggle by Frame (LFRAME)

GP0[10:8] : The highest 3 bits of the generator 0 period (POR = 100)
GP0[7:0] : The lower byte of the generator 0 period (POR = 00000000)

6.29 Set LCD Gen1

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	0	0	0	0	1	0	C2
Parameter 1	1	A_7	0	0	0	0	0	0	0	xx
Parameter 2	1	0	0	0	0	0	$GF1_2$	$GF1_1$	$GF1_0$	xx
Parameter 3	1	$GF1_7$	$GF1_6$	$GF1_5$	$GF1_4$	$GF1_3$	$GF1_2$	$GF1_1$	$GF1_0$	xx
Parameter 4	1	0	0	0	0	0	$GR1_2$	$GR1_1$	$GR1_0$	xx
Parameter 5	1	$GR1_7$	$GR1_6$	$GR1_5$	$GR1_4$	$GR1_3$	$GR1_2$	$GR1_1$	$GR1_0$	xx
Parameter 6	1	F_7	F_6	F_5	F_4	F_3	$GP1_2$	$GP1_1$	$GP1_0$	xx
Parameter 7	1	$GP1_7$	$GP1_6$	$GP1_5$	$GP1_4$	$GP1_3$	$GP1_2$	$GP1_1$	$GP1_0$	xx

6.30 Set LCD Gen2

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	0	0	0	1	0	0	C4
Parameter 1	1	A_7	0	0	0	0	0	0	0	xx
Parameter 2	1	0	0	0	0	0	$GF2_2$	$GF2_1$	$GF2_0$	xx
Parameter 3	1	$GF2_7$	$GF2_6$	$GF2_5$	$GF2_4$	$GF2_3$	$GF2_2$	$GF2_1$	$GF2_0$	xx
Parameter 4	1	0	0	0	0	0	$GR2_2$	$GR2_1$	$GR2_0$	xx
Parameter 5	1	$GR2_7$	$GR2_6$	$GR2_5$	$GR2_4$	$GR2_3$	$GR2_2$	$GR2_1$	$GR2_0$	xx
Parameter 6	1	F_7	F_6	F_5	F_4	F_3	$GP2_2$	$GP2_1$	$GP2_0$	xx
Parameter 7	1	$GP2_7$	$GP2_6$	$GP2_5$	$GP2_4$	$GP2_3$	$GP2_2$	$GP2_1$	$GP2_0$	xx

6.31 Set LCD Gen3

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	0	0	0	1	1	0	C6
Parameter 1	1	A_7	0	0	0	0	0	0	0	xx
Parameter 2	1	0	0	0	0	0	$GF3_2$	$GF3_1$	$GF3_0$	xx
Parameter 3	1	$GF3_7$	$GF3_6$	$GF3_5$	$GF3_4$	$GF3_3$	$GF3_2$	$GF3_1$	$GF3_0$	xx
Parameter 4	1	0	0	0	0	0	$GR3_2$	$GR3_1$	$GR3_0$	xx
Parameter 5	1	$GR3_7$	$GR3_6$	$GR3_5$	$GR3_4$	$GR3_3$	$GR3_2$	$GR3_1$	$GR3_0$	xx
Parameter 6	1	F_7	F_6	F_5	F_4	F_3	$GP3_2$	$GP3_1$	$GP3_0$	xx
Parameter 7	1	$GP3_7$	$GP3_6$	$GP3_5$	$GP3_4$	$GP3_3$	$GP3_2$	$GP3_1$	$GP3_0$	xx

6.32 Set DBC Configuration

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	0	1	0	0	0	0	D0
Parameter 1	1	0	A_6	A_5	0	A_3	A_2	0	A_0	xx

Description
Set the Dynamic Backlight Control configuration.

A[6] : DBC Manual Brightness enable (POR = 1)
0 Enable
1 Disable

A[5] : Transition effect (POR = 0)
0 Transition effect disable
1 Transition effect enable
Transition effect is used to remove visible backlight flickering. If rapid brightness change is required, it is recommended to enable this bit.

A[3:2] : Energy saving selection for DBC (POR = 00)
00 DBC is disable
01 Conservative mode
10 Normal mode
11 Aggressive mode

A[0] : Master enable of DBC (POR = 0)
0 DBC disable
1 DBC enable

6.33 Get Pixel Data Interface

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	1	1	0	0	0	0	F0
Parameter 1	1	0	0	0	0	0	A_2	A_1	A_0	xx

Description
Set the pixel data format to 8-bit / 9-bit / 12-bit / 16-bit / 16-bit(565) / 18-bit / 24-bit in the parallel host processor interface

A[2:0] : Pixel Data Interface Format (POR = 101)
000 8-bit
001 12-bit
010 16-bit packed
011 16-bit (565 format)
100 18-bit
101 24-bit
110 9-bit
Others Reserved

6.34 Set LSHIFT Frequency

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	1	0	0	1	1	0	E6
Parameter 1	1	0	0	0	0	$LCDC\_FPR_{19}$	$LCDC\_FPR_{18}$	$LCDC\_FPR_{17}$	$LCDC\_FPR_{16}$	xx
Parameter 2	1	$LCDC\_FPR_{15}$	$LCDC\_FPR_{14}$	$LCDC\_FPR_{13}$	$LCDC\_FPR_{12}$	$LCDC\_FPR_{11}$	$LCDC\_FPR_{10}$	$LCDC\_FPR_{9}$	$LCDC\_FPR_{8}$	xx
Parameter 3	1	$LCDC\_FPR_{7}$	$LCDC\_FPR_{6}$	$LCDC\_FPR_{5}$	$LCDC\_FPR_{4}$	$LCDC\_FPR_{3}$	$LCDC\_FPR_{2}$	$LCDC\_FPR_{1}$	$LCDC\_FPR_{0}$	xx

Description
Set the LSHIFT (pixel clock) frequency

LCDC_FPR[19:16] : The highest 4 bits for the pixel clock frequency settings. (POR = 0111)
LCDC_FPR[15:8] : The higher byte for the pixel clock frequency settings. (POR = 11111111)
LCDC_FPR[7:0] : The low byte for the pixel clock frequency settings. (POR = 11111111)

Configure the pixel clock to PLL freq x ((LCDC_FPR + 1) / 2^{20})

To obtain PCLK = 5.3MHz with PLL Frequency = 120MHz,
5.3MHz = 120MHz * LCDC_FPR / 2^{20}
LCDC_FPR = 46312

WRITE COMMAND "0xE6"
WRITE DATA "0x00" (LCDC_FPR = 46312)
WRITE DATA "0xB4"
WRITE DATA "0xE7"

6.35 Set Deep Sleep

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	1	0	0	1	0	1	E5

Set deep sleep mode. PLL would be stopped.
It needs to issue 2 dummy read to exit Deep Sleep mode.

6.36 Set PLL

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	1	0	0	0	0	0	E0
Parameter 1	1	0	0	0	0	0	0	A_1	A_0	xx

Description
Start the PLL. Before the start, the system was operated with the crystal oscillator or clock input.

A[1] : Lock PLL (POR = 0)
After PLL enabled for 100us, can start to lock PLL
0 Use reference clock as system clock
1 Use PLL output as system clock

A[0] : Enable PLL (POR = 0)
0 Disable PLL
1 Enable PLL

SSD1963 needed to switch to PLL output as system clock after PLL is locked. The following is the program sequence.
WRITE COMMAND "0xE0"
WRITE DATA "0x01"

Wait 100us to let the PLL stable
WRITE DATA “0x03”

6.37 Set PLL MN

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	1	1	1	0	0	0	1	0	E2
Parameter 1	1	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	xx
Parameter 2	1	0	0	0	0	M_3	M_2	M_1	M_0	xx
Parameter 3	1	0	0	0	0	0	C_2	0	0	xx

Description
Set the MN of PLL
N[7:0] : Multiplier (N) of PLL. (POR = 00101101)

M[3:0] : Divider (M) of PLL. (POR = 0011)

C[2] : Effectuate MN value (POR = 0)
0 Ignore the multiplier (N) and divider (M) values in A[7:0] and B[7:0]
1 Effectuate the multiplier and divider value

VCO = Reference input clock x N
PLL frequency = VCO / M

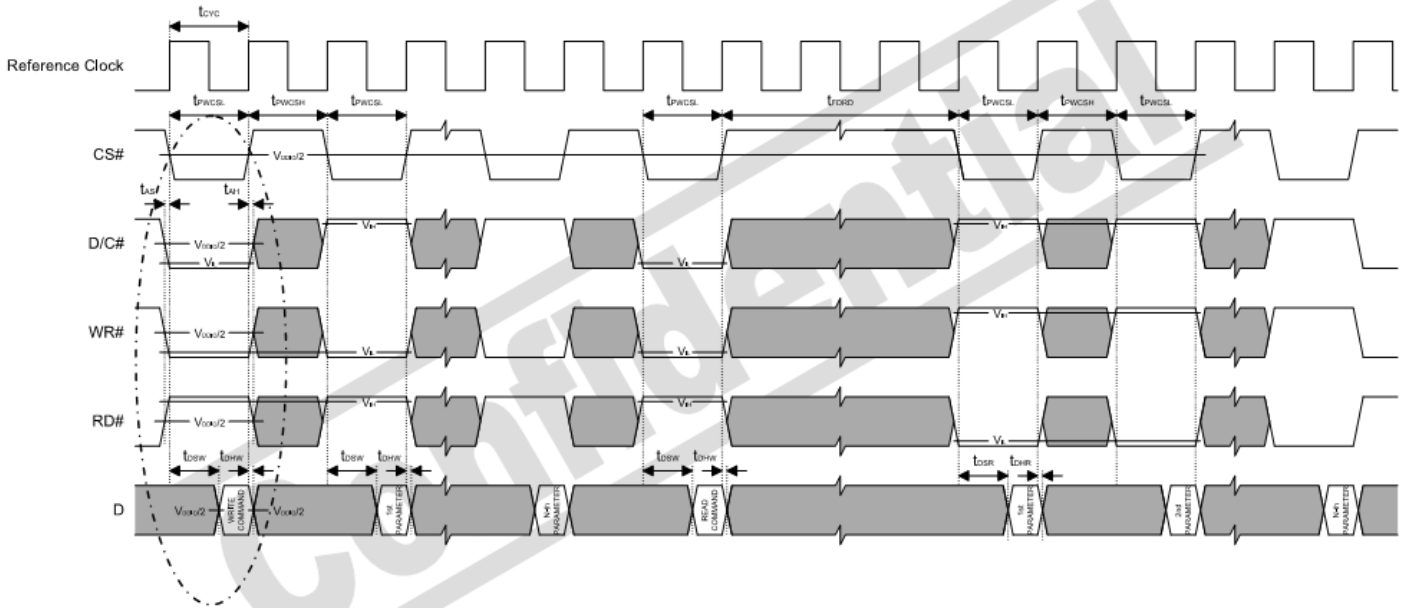
*** Note : 250MHz < VCO < 800MHz**

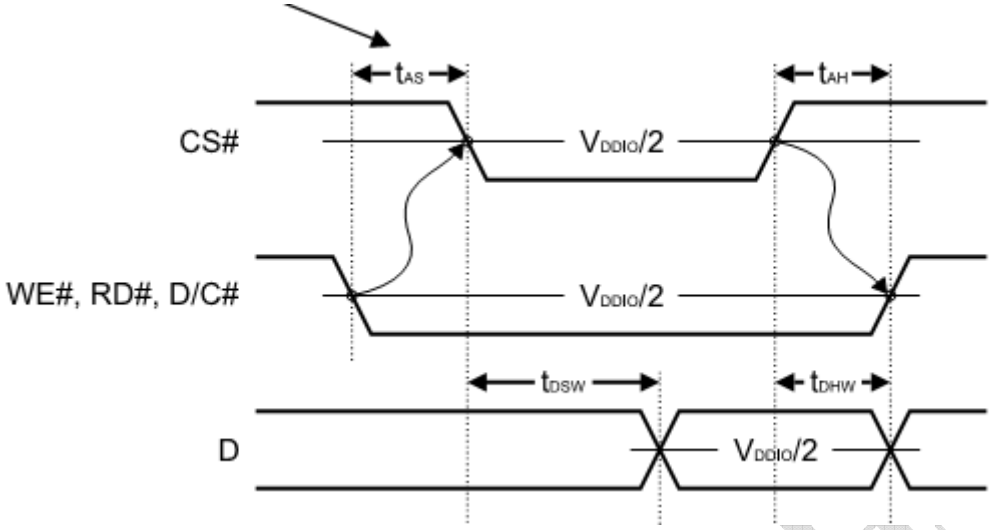
For a 10MHz reference clock to obtain 115MHz PLL frequency, user cannot program N = 23 and M = 2. The closet setting in this situation is setting N=34 and M=3, where 10 x 34 / 3 = 113.33MHz.

WRITE COMMAND “0xE2”
WRITE DATA “0x21” (N=34)
WRITE DATA “0x02” (M=3)
WRITE DATA “0x54” (Dummy Byte)

7. AC characteristics

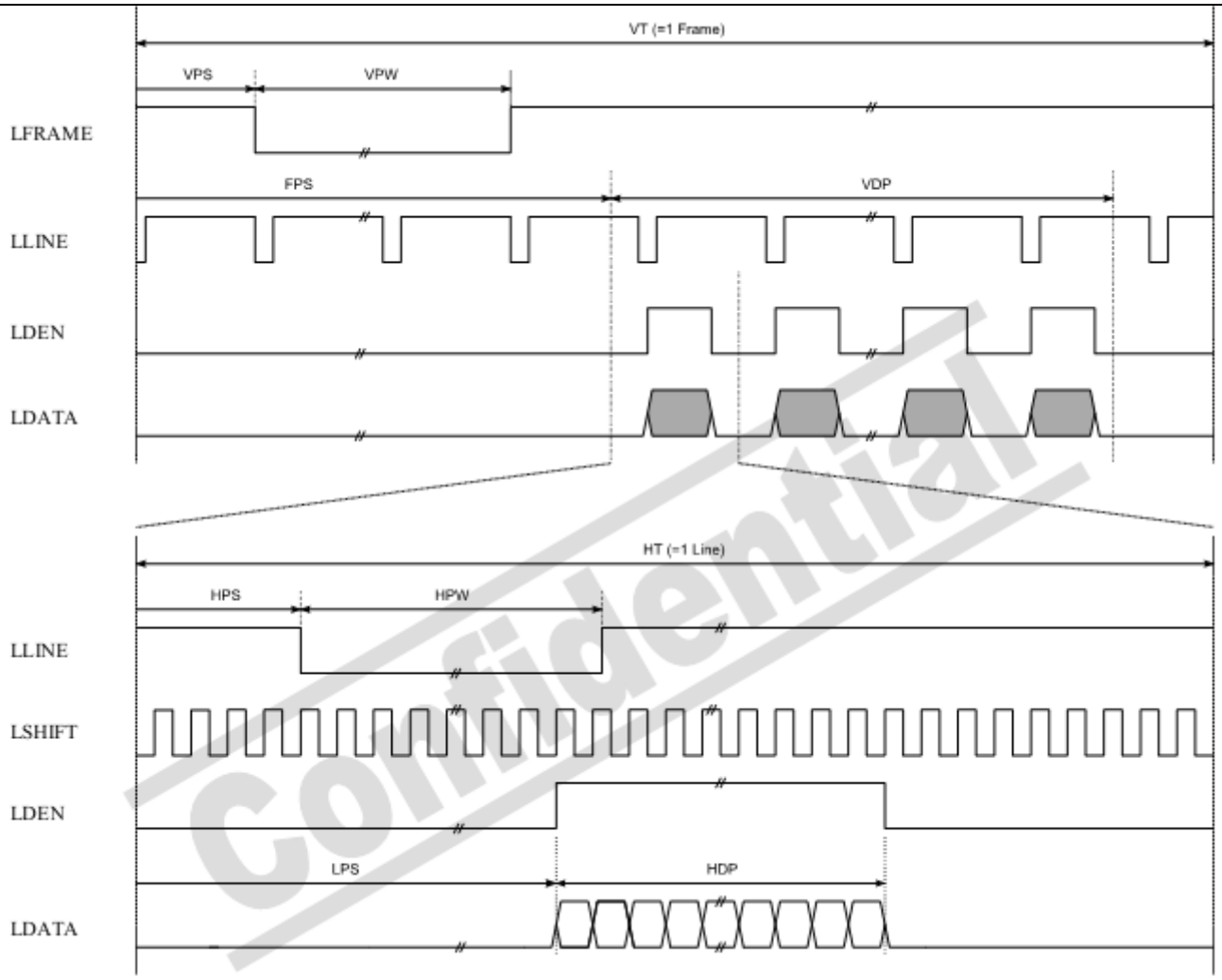
7.1 MCU Interface Timing(8080)



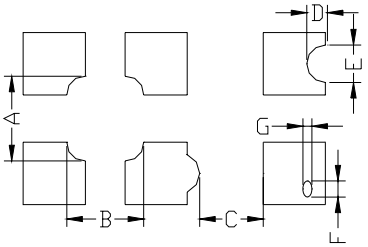


Symbol	Parameter	Min	Typ	Max	Unit
t_{cyc}	Reference Clock Cycle Time	9	-	-	ns
t_{PWCSL}	Pulse width CS# low	1	-	-	t_{CYC}
t_{PWCSH}	Pulse width CS# high	1	-	-	t_{CYC}
t_{FDRD}	First Read Data Delay	5	-	-	t_{CYC}
t_{AS}	Address Setup Time	1	-	-	ns
t_{AH}	Address Hold Time	1	-	-	ns
t_{DSW}	Data Setup Time	4	-	-	ns
t_{DHW}	Data Hold Time	1	-	-	ns
t_{DSR}	Data Access Time	-	-	5	ns
t_{DHR}	Output Hold time	1	-	-	ns

7.2 LCD Interface Timing



8 Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2}\leq 0.28$ | $0<C$ | $\frac{D+E}{2}\leq 0.25$ | $\frac{F+G}{2}\leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball,	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm)	Minor

solder hips)	(3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	
16) Bezel flaw	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

9. Handling Precautions

9.1 Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

9.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

-Isopropyl alcohol

-Ethyl alcohol

-Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

-Water

-Ketene

-Aromatics

9.3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

9.4 Packaging

-Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

-To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

9.5 Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.

-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

9.6 Storage

In the case of storing for a long period of time, the following ways are recommended:

-Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.

-Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.

-Storing with no touch on polarizer surface by any thing else.

9.7 Safety

-It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.

10. Packaging Specifications

TBD