SSD1848

Advanced Information

130 x 130 STN
LCD Segment / Common 4G/S Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

CONTENTS

TABLES

FIGURES

GENERAL DESCRIPTION

SSD1848 is a single-chip CMOS LCD driver with controller for dot-matrix graphic liquid crystal display system. SSD1848 consists of 260 high-voltage driving output pins for driving maximum 130 Segments, 130 Commons.

SSD1848 consists of 130 x 130 x 2 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from common MCU through 8-bit 6800-series / 8080-series compatible Parallel Interface or 3-wires / 4-wires Serial Peripheral Interface by software program selections.

SSD1848 embeds DC-DC Converter, On-Chip Oscillator and Bias Divider to reduce the number of external components. With the advance design, low power consumption, stable LCD operating voltage and flexible die package layout, SSD1848 is suitable for any portable battery-driven applications requiring long operation period with compact size.

1 FEATURES

- Power Supply:
  - V_{DD} = 2.4V – 3.3V
  - V_{DDIO} = 1.7V – V_{DD}
  - V_{CI} = V_{DD} – 3.3V
- LCD Driving Output Voltage: max. V_{OUT} = +15V
- Maximum display size: 130 columns by 130 rows
- 8-bit 6800-series / 8080-series Parallel Interface, 3-wires and 4-wires Serial Peripheral Interface
- On-Chip 130 x 130 x 2 = 33,800 bits Graphic Display Data RAM
- Column Re-mapping and RAM Page scan direction control
- Vertical Scrolling by Common
- On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
- Software selectable 4X / 5X / 6X / 7X On-Chip DC-DC Converter
- Programmable LCD Driving Voltage Temperature Compensation Coefficients
- On-Chip Bias Divider with internal compensation capacitors (except V_{OUT})
- Programmable multiplex ratio: 1/16 to 1/128 and1/130
- Programmable bias ratio: 1/4, 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11, 1/12, 1/13
- Display Offset Control
- Dual Level Non-Volatile Memory (OTP) for V_{OUT} calibration
- N-line inversion
- 64 Levels Internal Contrast Control

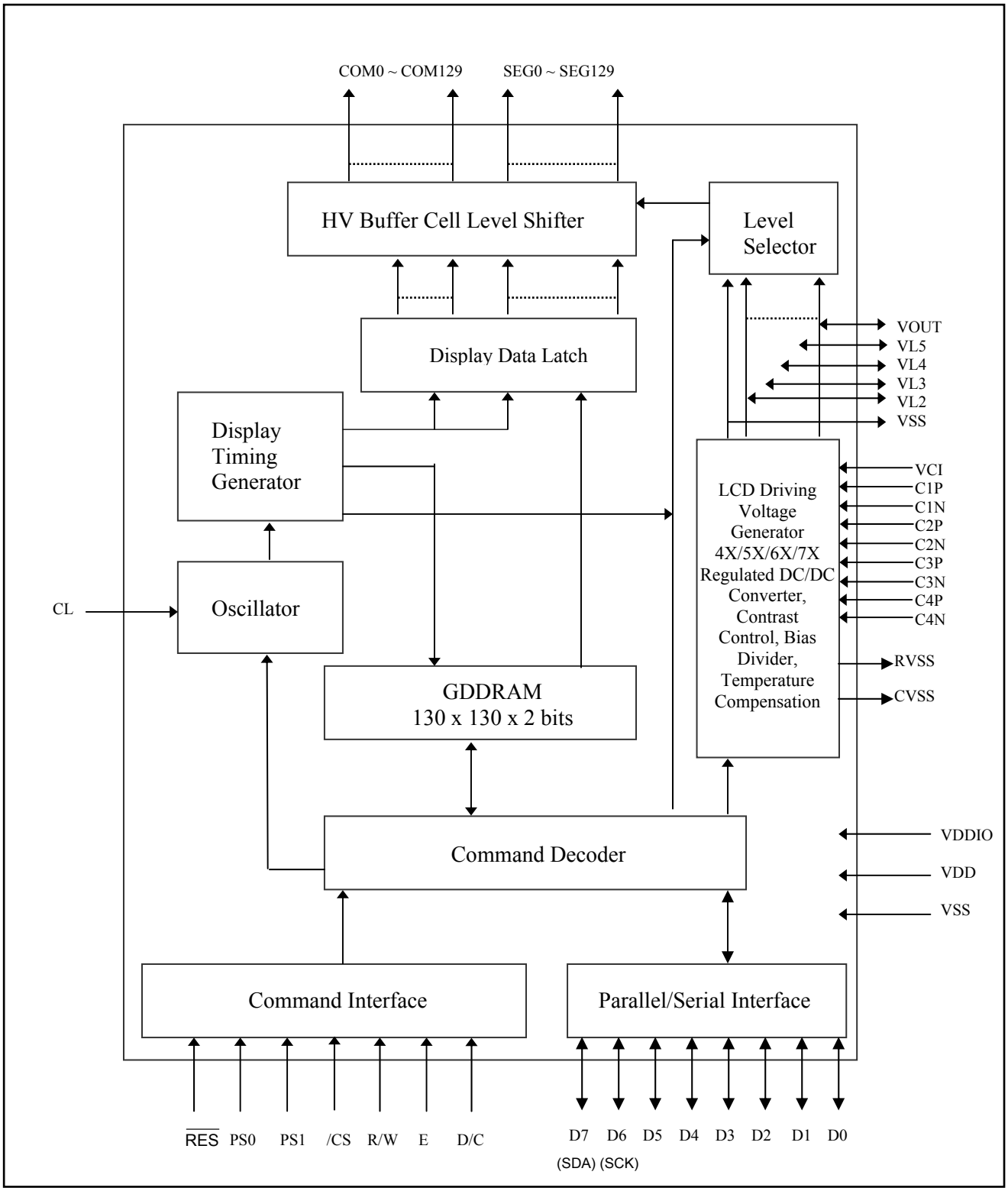
2 ORDERING INFORMATION

Table 2-1: Ordering Information

Ordering Part Number	Package Form	Reference	Remark
SSD1848Z	Gold Bump Die		
SSD1848U	COF		

4 BLOCK DIAGRAM

Figure 4-1: SSD1848 Block Diagram

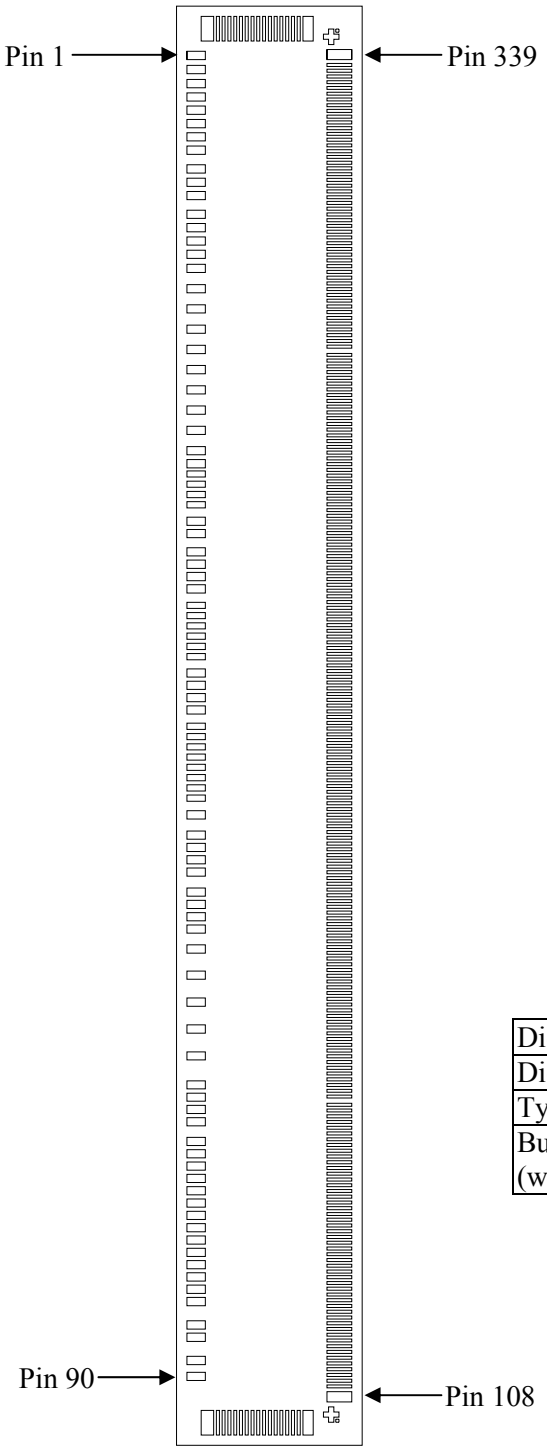


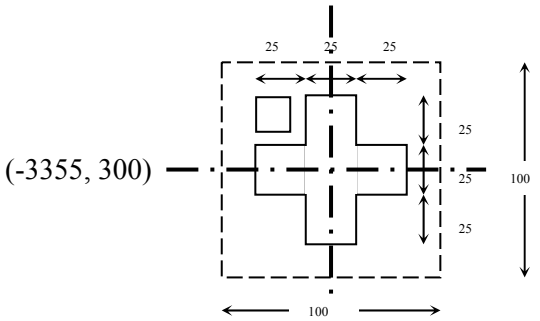
5 DIE PAD FLOOR PLAN

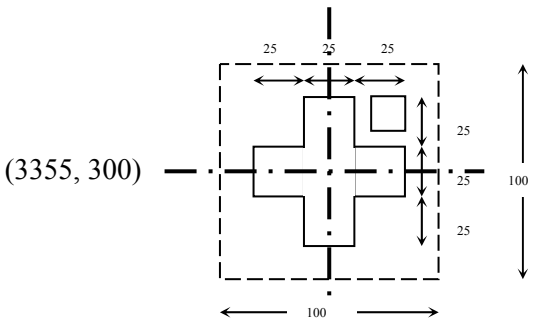
Figure 5-1: SSD1848 Die Pad Floor Plan

Note

(1) Diagram showing the die face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold bump.
(5) IC material Temperature expansion factor should take into account







Die Size	7.020x0.910=6.388mm^2
Die Thickness	300 ± 25 um
Typical Bump Height	15 um
Bump Co-planarity (within die)	<=2 um

Table 5-1: SSD1848 Bump Die Pad Coordinates (Bump center)

Pad #	Pin Name	X / um	Y / um	Pad #	Pin Name	X / um	Y / um
1	DUMMY	-3264.40	-354.50	49	NC	103.00	-354.50
2	CL	-3195.80	-354.50	50	NC	153.00	-354.50
3	VSS	-3127.20	-354.50	51	NC	203.00	-354.50
4	PS0	-3062.30	-354.50	52	NC	253.00	-354.50
5	VDDIO	-2997.40	-354.50	53	NC	303.00	-354.50
6	PS1	-2932.50	-354.50	54	NC	353.00	-354.50
7	VSS	-2867.60	-354.50	55	RVSS	434.40	-354.50
8	/CS	-2802.70	-354.50	56	VSS	533.10	-354.50
9	/RES	-2711.50	-354.50	57	VSS	593.10	-354.50
10	VDDIO	-2646.60	-354.50	58	VSS	653.10	-354.50
11	D/C	-2581.70	-354.50	59	VSS	713.10	-354.50
12	R/W	-2490.50	-354.50	60	CVSS	810.20	-354.50
13	VSS	-2425.60	-354.50	61	CVSS	870.20	-354.50
14	E	-2360.70	-354.50	62	CVSS	930.20	-354.50
15	VDDIO	-2295.80	-354.50	63	CVSS	990.20	-354.50
16	D0	-2227.10	-354.50	64	VL2	1087.30	-354.50
17	D1	-2128.50	-354.50	65	VL3	1215.10	-354.50
18	D2	-2029.90	-354.50	66	VL4	1346.10	-354.50
19	D3	-1931.30	-354.50	67	VL5	1477.10	-354.50
20	D4	-1832.70	-354.50	68	ATEST	1608.10	-354.50
21	D5	-1734.10	-354.50	69	VOUT	1749.10	-354.50
22	D6	-1635.50	-354.50	70	VOUT	1809.10	-354.50
23	D6	-1536.90	-354.50	71	VOUT	1869.10	-354.50
24	D7	-1438.30	-354.50	72	VOUT	1929.10	-354.50
25	D7	-1339.70	-354.50	73	C4P	2024.60	-354.50
26	VSS	-1276.00	-354.50	74	C4P	2084.60	-354.50
27	NC	-1226.00	-354.50	75	C4N	2144.60	-354.50
28	NC	-1176.00	-354.50	76	C4N	2204.60	-354.50
29	NC	-1126.00	-354.50	77	C3P	2264.60	-354.50
30	NC	-1076.00	-354.50	78	C3P	2324.60	-354.50
31	VDDIO	-995.60	-354.50	79	C3N	2384.60	-354.50
32	VDDIO	-935.60	-354.50	80	C3N	2444.60	-354.50
33	VDD	-846.60	-354.50	81	C2P	2504.60	-354.50
34	VDD	-786.60	-354.50	82	C2P	2564.60	-354.50
35	VDD	-726.60	-354.50	83	C2N	2624.60	-354.50
36	VDD	-666.60	-354.50	84	C2N	2684.60	-354.50
37	NC	-586.20	-354.50	85	C1P	2744.60	-354.50
38	NC	-536.20	-354.50	86	C1P	2804.60	-354.50
39	NC	-486.20	-354.50	87	C1N	2918.20	-354.50
40	VSS	-436.20	-354.50	88	C1N	2978.20	-354.50
41	NC	-386.20	-354.50	89	DUMMY	3091.60	-354.50
42	NC	-336.20	-354.50	90	DUMMY	3168.95	-354.50
43	VCI	-256.80	-354.50	91	DUMMY	3394.45	-299.77
44	VCI	-196.80	-354.50	92	COM0	3394.45	-249.27
45	VCI	-136.80	-354.50	93	COM1	3394.45	-221.27
46	VCI	-76.80	-354.50	94	COM2	3394.45	-193.27
47	NC	3.00	-354.50	95	COM3	3394.45	-165.27
48	NC	53.00	-354.50	96	COM4	3394.45	-137.27

Pad #	Pin Name	X / um	Y / um	Pad #	Pin Name	X / um	Y / um
97	COM5	3394.45	-109.27	145	COM51	2210.00	339.50
98	COM6	3394.45	-81.27	146	COM52	2182.00	339.50
99	COM7	3394.45	-53.27	147	COM53	2154.00	339.50
100	COM8	3394.45	-25.27	148	COM54	2126.00	339.50
101	COM9	3394.45	2.73	149	COM55	2098.00	339.50
102	COM10	3394.45	30.73	150	COM56	2070.00	339.50
103	COM11	3394.45	58.73	151	COM57	2042.00	339.50
104	COM12	3394.45	86.73	152	COM58	2014.00	339.50
105	COM13	3394.45	114.73	153	COM59	1986.00	339.50
106	COM14	3394.45	142.73	154	COM60	1958.00	339.50
107	DUMMY	3394.45	188.23	155	COM61	1930.00	339.50
108	DUMMY	3268.50	339.50	156	COM62	1902.00	339.50
109	COM15	3218.00	339.50	157	COM63	1874.00	339.50
110	COM16	3190.00	339.50	158	COM64	1846.00	339.50
111	COM17	3162.00	339.50	159	SEG129	1806.00	339.50
112	COM18	3134.00	339.50	160	SEG128	1778.00	339.50
113	COM19	3106.00	339.50	161	SEG127	1750.00	339.50
114	COM20	3078.00	339.50	162	SEG126	1722.00	339.50
115	COM21	3050.00	339.50	163	SEG125	1694.00	339.50
116	COM22	3022.00	339.50	164	SEG124	1666.00	339.50
117	COM23	2994.00	339.50	165	SEG123	1638.00	339.50
118	COM24	2966.00	339.50	166	SEG122	1610.00	339.50
119	COM25	2938.00	339.50	167	SEG121	1582.00	339.50
120	COM26	2910.00	339.50	168	SEG120	1554.00	339.50
121	COM27	2882.00	339.50	169	SEG119	1526.00	339.50
122	COM28	2854.00	339.50	170	SEG118	1498.00	339.50
123	COM29	2826.00	339.50	171	SEG117	1470.00	339.50
124	COM30	2798.00	339.50	172	SEG116	1442.00	339.50
125	COM31	2770.00	339.50	173	SEG115	1414.00	339.50
126	COM32	2742.00	339.50	174	SEG114	1386.00	339.50
127	COM33	2714.00	339.50	175	SEG113	1358.00	339.50
128	COM34	2686.00	339.50	176	SEG112	1330.00	339.50
129	COM35	2658.00	339.50	177	SEG111	1302.00	339.50
130	COM36	2630.00	339.50	178	SEG110	1274.00	339.50
131	COM37	2602.00	339.50	179	SEG109	1246.00	339.50
132	COM38	2574.00	339.50	180	SEG108	1218.00	339.50
133	COM39	2546.00	339.50	181	SEG107	1190.00	339.50
134	COM40	2518.00	339.50	182	SEG106	1162.00	339.50
135	COM41	2490.00	339.50	183	SEG105	1134.00	339.50
136	COM42	2462.00	339.50	184	SEG104	1106.00	339.50
137	COM43	2434.00	339.50	185	SEG103	1078.00	339.50
138	COM44	2406.00	339.50	186	SEG102	1050.00	339.50
139	COM45	2378.00	339.50	187	SEG101	1022.00	339.50
140	COM46	2350.00	339.50	188	SEG100	994.00	339.50
141	COM47	2322.00	339.50	189	SEG99	966.00	339.50
142	COM48	2294.00	339.50	190	SEG98	938.00	339.50
143	COM49	2266.00	339.50	191	SEG97	910.00	339.50
144	COM50	2238.00	339.50	192	SEG96	882.00	339.50

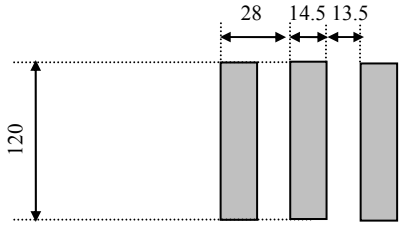
Pad #	Pin Name	X / um	Y / um	Pad #	Pin Name	X / um	Y / um
193	SEG95	854.00	339.50	241	SEG47	-490.00	339.50
194	SEG94	826.00	339.50	242	SEG46	-518.00	339.50
195	SEG93	798.00	339.50	243	SEG45	-546.00	339.50
196	SEG92	770.00	339.50	244	SEG44	-574.00	339.50
197	SEG91	742.00	339.50	245	SEG43	-602.00	339.50
198	SEG90	714.00	339.50	246	SEG42	-630.00	339.50
199	SEG89	686.00	339.50	247	SEG41	-658.00	339.50
200	SEG88	658.00	339.50	248	SEG40	-686.00	339.50
201	SEG87	630.00	339.50	249	SEG39	-714.00	339.50
202	SEG86	602.00	339.50	250	SEG38	-742.00	339.50
203	SEG85	574.00	339.50	251	SEG37	-770.00	339.50
204	SEG84	546.00	339.50	252	SEG36	-798.00	339.50
205	SEG83	518.00	339.50	253	SEG35	-826.00	339.50
206	SEG82	490.00	339.50	254	SEG34	-854.00	339.50
207	SEG81	462.00	339.50	255	SEG33	-882.00	339.50
208	SEG80	434.00	339.50	256	SEG32	-910.00	339.50
209	SEG79	406.00	339.50	257	SEG31	-938.00	339.50
210	SEG78	378.00	339.50	258	SEG30	-966.00	339.50
211	SEG77	350.00	339.50	259	SEG29	-994.00	339.50
212	SEG76	322.00	339.50	260	SEG28	-1022.00	339.50
213	SEG75	294.00	339.50	261	SEG27	-1050.00	339.50
214	SEG74	266.00	339.50	262	SEG26	-1078.00	339.50
215	SEG73	238.00	339.50	263	SEG25	-1106.00	339.50
216	SEG72	210.00	339.50	264	SEG24	-1134.00	339.50
217	SEG71	182.00	339.50	265	SEG23	-1162.00	339.50
218	SEG70	154.00	339.50	266	SEG22	-1190.00	339.50
219	SEG69	126.00	339.50	267	SEG21	-1218.00	339.50
220	SEG68	98.00	339.50	268	SEG20	-1246.00	339.50
221	SEG67	70.00	339.50	269	SEG19	-1274.00	339.50
222	SEG66	42.00	339.50	270	SEG18	-1302.00	339.50
223	SEG65	14.00	339.50	271	SEG17	-1330.00	339.50
224	SEG64	-14.00	339.50	272	SEG16	-1358.00	339.50
225	SEG63	-42.00	339.50	273	SEG15	-1386.00	339.50
226	SEG62	-70.00	339.50	274	SEG14	-1414.00	339.50
227	SEG61	-98.00	339.50	275	SEG13	-1442.00	339.50
228	SEG60	-126.00	339.50	276	SEG12	-1470.00	339.50
229	SEG59	-154.00	339.50	277	SEG11	-1498.00	339.50
230	SEG58	-182.00	339.50	278	SEG10	-1526.00	339.50
231	SEG57	-210.00	339.50	279	SEG9	-1554.00	339.50
232	SEG56	-238.00	339.50	280	SEG8	-1582.00	339.50
233	SEG55	-266.00	339.50	281	SEG7	-1610.00	339.50
234	SEG54	-294.00	339.50	282	SEG6	-1638.00	339.50
235	SEG53	-322.00	339.50	283	SEG5	-1666.00	339.50
236	SEG52	-350.00	339.50	284	SEG4	-1694.00	339.50
237	SEG51	-378.00	339.50	285	SEG3	-1722.00	339.50
238	SEG50	-406.00	339.50	286	SEG2	-1750.00	339.50
239	SEG49	-434.00	339.50	287	SEG1	-1778.00	339.50
240	SEG48	-462.00	339.50	288	SEG0	-1806.00	339.50

Pad #	Pin Name	X / um	Y / um	Pad #	Pin Name	X / um	Y / um
289	COM65	-1846.00	339.50	337	COM113	-3190.00	339.50
290	COM66	-1874.00	339.50	338	COM114	-3218.00	339.50
291	COM67	-1902.00	339.50	339	DUMMY	-3268.50	339.50
292	COM68	-1930.00	339.50	340	DUMMY	-3394.45	188.23
293	COM69	-1958.00	339.50	341	COM115	-3394.45	142.73
294	COM70	-1986.00	339.50	342	COM116	-3394.45	114.73
295	COM71	-2014.00	339.50	343	COM117	-3394.45	86.73
296	COM72	-2042.00	339.50	344	COM118	-3394.45	58.73
297	COM73	-2070.00	339.50	345	COM119	-3394.45	30.73
298	COM74	-2098.00	339.50	346	COM120	-3394.45	2.73
299	COM75	-2126.00	339.50	347	COM121	-3394.45	-25.27
300	COM76	-2154.00	339.50	348	COM122	-3394.45	-53.27
301	COM77	-2182.00	339.50	349	COM123	-3394.45	-81.27
302	COM78	-2210.00	339.50	350	COM124	-3394.45	-109.27
303	COM79	-2238.00	339.50	351	COM125	-3394.45	-137.27
304	COM80	-2266.00	339.50	352	COM126	-3394.45	-165.27
305	COM81	-2294.00	339.50	353	COM127	-3394.45	-193.27
306	COM82	-2322.00	339.50	354	COM128	-3394.45	-221.27
307	COM83	-2350.00	339.50	355	COM129	-3394.45	-249.27
308	COM84	-2378.00	339.50	356	DUMMY	-3394.45	-299.77
309	COM85	-2406.00	339.50				
310	COM86	-2434.00	339.50				
311	COM87	-2462.00	339.50				
312	COM88	-2490.00	339.50				
313	COM89	-2518.00	339.50				
314	COM90	-2546.00	339.50				
315	COM91	-2574.00	339.50				
316	COM92	-2602.00	339.50				
317	COM93	-2630.00	339.50				
318	COM94	-2658.00	339.50				
319	COM95	-2686.00	339.50				
320	COM96	-2714.00	339.50				
321	COM97	-2742.00	339.50				
322	COM98	-2770.00	339.50				
323	COM99	-2798.00	339.50				
324	COM100	-2826.00	339.50				
325	COM101	-2854.00	339.50				
326	COM102	-2882.00	339.50				
327	COM103	-2910.00	339.50				
328	COM104	-2938.00	339.50				
329	COM105	-2966.00	339.50				
330	COM106	-2994.00	339.50				
331	COM107	-3022.00	339.50				
332	COM108	-3050.00	339.50				
333	COM109	-3078.00	339.50				
334	COM110	-3106.00	339.50				
335	COM111	-3134.00	339.50				
336	COM112	-3162.00	339.50				

Min. Pad Pitch	28um
Bump Size	1,740um^2
Bump Width Tolerance	± 2um

Bump Size		
Pad #	X [um]	Y [um]
1-26, 31-36, 43-46, 55-90	40	89
27-30, 37- 42, 47-54	30	89
91, 356	120	60
92-106, 341-355	120	14.5
107, 340	120	50
108, 339	50	120
109-338	14.5	120

Output Pad Pitch (um)



6 PIN DESCRIPTIONS

6.1 $\overline{\text{RES}}$

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

6.2 PS0, PS1

PS0 and PS1 determine the interface protocol between the driver and MCU. Refer to the following table for details.

PS0	PS1	Interface
L	L	3-wire SPI (write only)
L	H	4-wire SPI (write only)
H	L	8080 parallel interface (read and write allowed)
H	H	6800 parallel interface (read and write allowed)

Note: The above H refers to either VDDIO while L refers VSS

6.3 $\overline{\text{CS}}$

This pin is chip select input. The chip is enabled for display data/command transfer only when $\overline{\text{CS}}$ is low. A capacitor is suggested to be added between $\overline{\text{CS}}$ and VSS for noise filtering when necessary.

6.4 D/$\overline{\text{C}}$

This input pin is to identify display data/command cycle. When the pin is high, the data written to the driver will be written into display RAM. When the pin is low, the data will be interpreted as command.
This pin must be connected to VSS when 3-lines SPI interface is used.

6.5 R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as Read/Write (R/$\overline{\text{W}}$) selection input. Read mode will be carried out when this pin is pulled high and write mode when this pin is pulled low.
When 8080 interface mode is selected, this pin is the Write ($\overline{\text{WR}}$) control signal input. Data write operation is initiated when this pin is pulled low and the chip is selected.

6.6 E($\overline{\text{RD}}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/ write operation is initiated when this pin is pulled high and the chip is selected.

When 8080 interface mode is selected, this pin is the Read ($\overline{\text{RD}}$) control signal input. Data read operation is initiated when this pin is pulled low and the chip is selected.

6.7 D0-D7

These pins are 8-bit bi-directional data/command bus to be connected to the microprocessor's data bus. When serial mode is selected, D7 is the serial data input SDA, D6 is the serial clock input SCK and D0~D5 should be connected to VDDIO.

6.8 VDDIO

This pin is the system power supply pin of bus IO buffer. Please refer to Figure 13-4 on page 57 for connection example.

6.9 VDD

This pin is the system power supply pin of the logic block.

6.10 VSS

This is a logic ground pin. It must connect to GND from external supply.

6.11 VCI

Reference voltage input for internal DC-DC converter. The voltage of generated VOUT equals to the multiple factor (4X, 5X, 6X or 7X) times VCI with respect to VSS.
Note: voltage at this input pin must be larger than or equal to VDD.

6.12 RVSS

This pin is the ground for internal voltage regulator. It must connect to GND from external supply.

6.13 CVSS

This is an analog ground pin. It must connect to GND from external supply.

6.14 C1P, C1N, C2P, C2N, C3P, C3N, C4P, C4N

Connect an external capacitor to these pins when 4X, 5X, 6X or 7X DC-DC Converter Factor is set. Please refer to Figure 13-3 for booster configuration.

6.15 VOUT

This pin is the most positive LCD driving voltage. It can be supplied externally or generated by the internal regulator.

6.16 VL5, VL4, VL3 and VL2

These are LCD driving voltages. These pins should NOT be connected to any signal pins nor shorted together. They should be left open. They have the following relationship:
VOUT > VL5 > VL4 > VL3 > VL2 > VSS

	1:a bias
VL5	(a-1)/a*VOUT
VL4	(a-2)/a*VOUT
VL3	2/a*VOUT
VL2	1/a*VOUT

6.17 COM0 – COM129

These pins provide the row driving signal COM0 – COM129 to the LCD panel.

6.18 SEG0 – SEG129

These pins provide the column driving signal SEG0 – SEG129. Their voltage level is VSS during sleep mode and standby mode.

6.19 CL

This pin is the external clock input (The logic high value is VDDIO) for the device if external clock mode is selected by software command. Under POR operation, this pin should be left opened and internal oscillator will be used after power on reset.

6.20 NC

These No Connection pins should NOT be connected to any signal pins nor shorted together. They should be left open.

6.21 DUMMY

This pin is a floating dummy pin with no internal circuit connection.

6.22 ATEST

Test pin. No connection for this pin.

6.23 Microprocessor Interface Logic

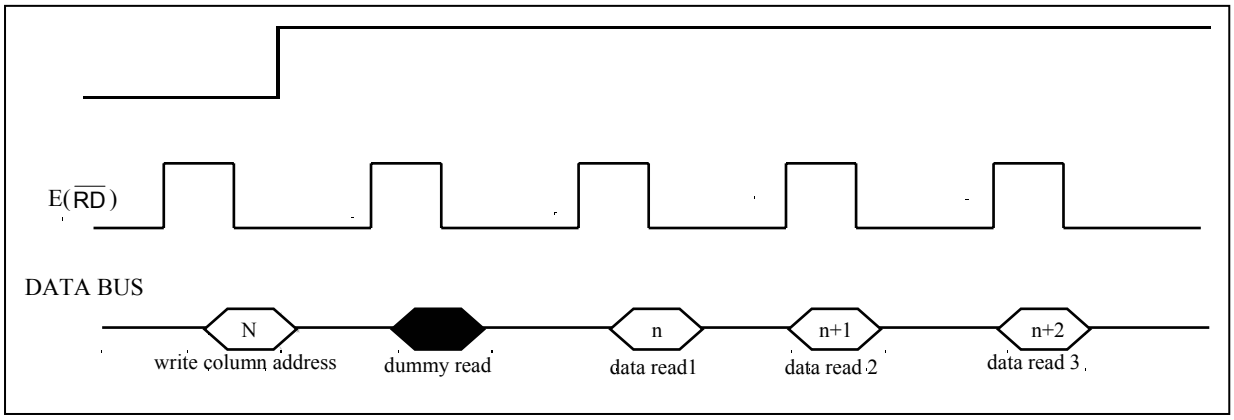
The Microprocessor Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS0 to PS1 pins. Please refer to the pin descriptions on page 14.

MPU Parallel 6800-series Interface

The parallel Interface consists of 8 bi-directional data pins (D_7 – D_0), R/$\overline{W}$, D/$\overline{C}$, E, $\overline{CS}$. R/$\overline{W}$ ($\overline{WR}$) input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. R/$\overline{W}$ input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E input serves as data latch signal (clock) when high provided that $\overline{CS}$ is low. Please refer to Figure 12-1 on page 52 for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following figure.

Figure 6-1: Display Data



MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins D7 – D0, $\overline{RD}$, $\overline{WR}$, D/$\overline{C}$, $\overline{CS}$. $\overline{RD}$ input serves as data read latch signal (clock) when low provided that $\overline{CS}$ is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by D/$\overline{C}$. $\overline{WR}$ input serves as data write latch signal (clock) when low provided that $\overline{CS}$ is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by D/$\overline{C}$. A dummy read is also required before the first actual display data read for 8080-series interface. Please refer to Figure 12-2 on page 53 for Parallel Interface Timing Diagram of 8080-series microprocessors

MPU 4-wires Serial Peripheral Interface

The 4-wires serial peripheral Interface consists of serial clock SCK, serial data SDA, D/$\overline{C}$, $\overline{CS}$. SDA is shifted into 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6 …… data bit 0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock. Please refer to Figure 12-3 on page 54 for 4-wires serial interface timing.

MPU 3-wires Serial Peripheral Interface

The operation is similar to 4-wires serial peripheral interface while $D/\overline{C}$ is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: $D/\overline{C}$ bit, D7 to D0 bit. The $D/\overline{C}$ bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM ($D/\overline{C}$ bit = 1) or the command register ($D/\overline{C}$ bit = 0). Please refer to Figure 12-4 on page 55 for 3-wires serial interface timing.

6.24 Reset Circuit

This block is integrated into the Microprocessor Interface Logic which includes Power On Reset circuitry and the hardware reset pin, $\overline{RES}$. Both of these having the same reset function. Once the $\overline{RES}$ pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10us. The status of the chip after reset is given by:

When $\overline{RES}$ input is low, the chip is initialized to the following:

1.	Display ON/OFF:	Display is OFF
2.	Normal/Inverse Display:	Normal Display
3.	COM Scan Direction:	COM0 → COM129
4.	Internal Oscillator:	Disable
5.	Reference Voltage Generation Circuit:	Disable
6.	Voltage regulator and Voltage Follower:	Disable
7.	Booster level:	6X
8.	Bias ratio:	1/13
9.	Multiplex ratio:	130 Mux
10.	Contrast Level:	20hex
11.	Internal regulator gain:	3.38(IRS=0)
12.	Average temperature gradient:	TC0
13.	Partial display mode:	Disable
	Start COM address:	0
	End COM address:	0
14.	Area Scroll set	
	Top block address:	0
	Bottom block address:	0
	Number of specified block:	0
	Area scroll mode:	Whole screen scroll mode
15.	Scroll start set	
	Start block address:	0
16.	Data Scan Direction	
	Normal/inverse display of page address:	Normal
	Normal/inverse display of column address:	Normal
	Address-scan direction:	Column direction
	Grayscale setup:	PWM (0%, 33%, 66%, 100%)
17.	Start Page Address set:	0
18.	End Page Address set:	0
19.	Start Column address set:	0
20.	End Column address set:	0

6.25 Command Decoder

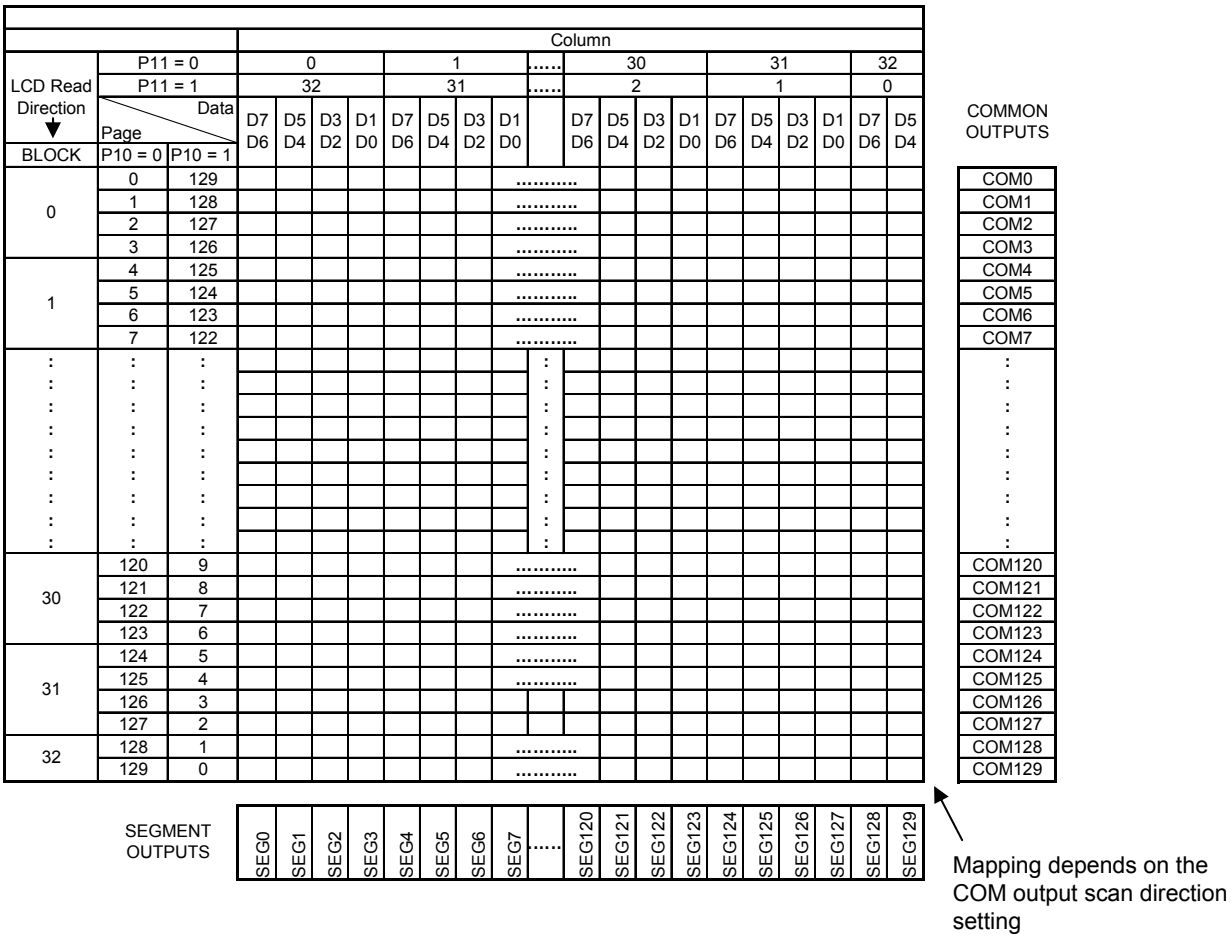
This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the $D/\overline{C}$ pin. If $D/\overline{C}$ pin is high, data is written to Graphic Display data RAM (GDDRAM). If it is low, the input at $D_7 – D_0$ is interpreted as a Command and it will be decoded. The decoded command will be written to the corresponding command register.

6.26 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 130 x 130 x 2 = 33,800bits. Figure 6-2on page 19 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command "Data Output/Scan direction" for detail description.

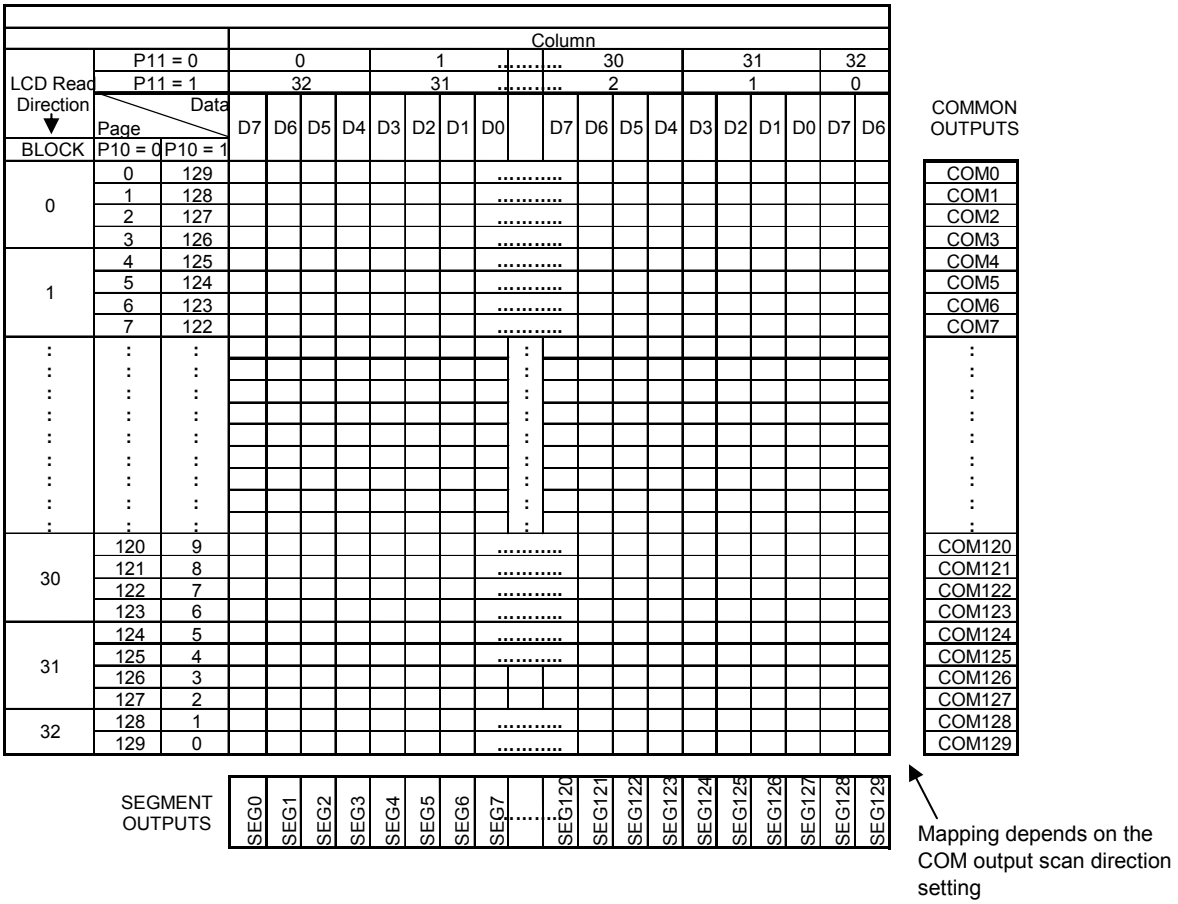
Four pages of display data form a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command "Set area Scroll" and "Set Scroll Start".

Figure 6-2: Graphic Display Data RAM (GDDRAM) Address Map for SSD1848 (GS mode)



Notes: Page and SEG data scan direction depend on data output scan direction setting
Data output scan direction setting cannot affect block scan direction

Figure 6-3: Graphic Display Data RAM (GDDRAM) Address Map for SSD1848 (B&W mode)



Notes: Page and SEG data scan direction depend on data output scan direction setting
Data output scan direction setting cannot affect block scan direction

6.27 LCD Driving Voltage Generator and Regulator

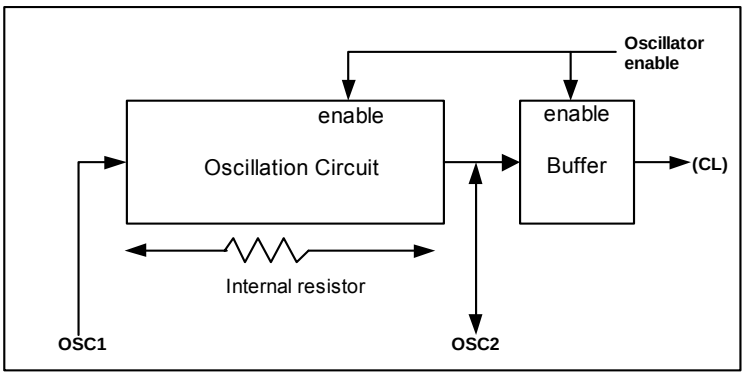
This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages. It consists of:

1. 4X, 5X, 6X and 7X DC-DC voltage converter.
2. Bias Divider - If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (VOUT) to give the LCD driving levels (VL2 - VL5).
3. Contrast Control -Software control of 64 voltage levels of LCD voltage.
4. Bias Ratio Selection circuitry -Software control of 1/4 to 1/13 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry - Provide 2 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is –0.01%.

6.28 Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 6-4). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

Figure 6-4: Oscillator structural block diagram



6.29 Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

6.30 HV Buffer Cell (Level Shifter)

This block is embedded in the Segment/Common Driver Circuits. HV Buffer Cell works as a level shifter, which translates the low voltage output signal to the required driving voltage. The output is shifted out with reference to the internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector, which is synchronized with the internal M signal.

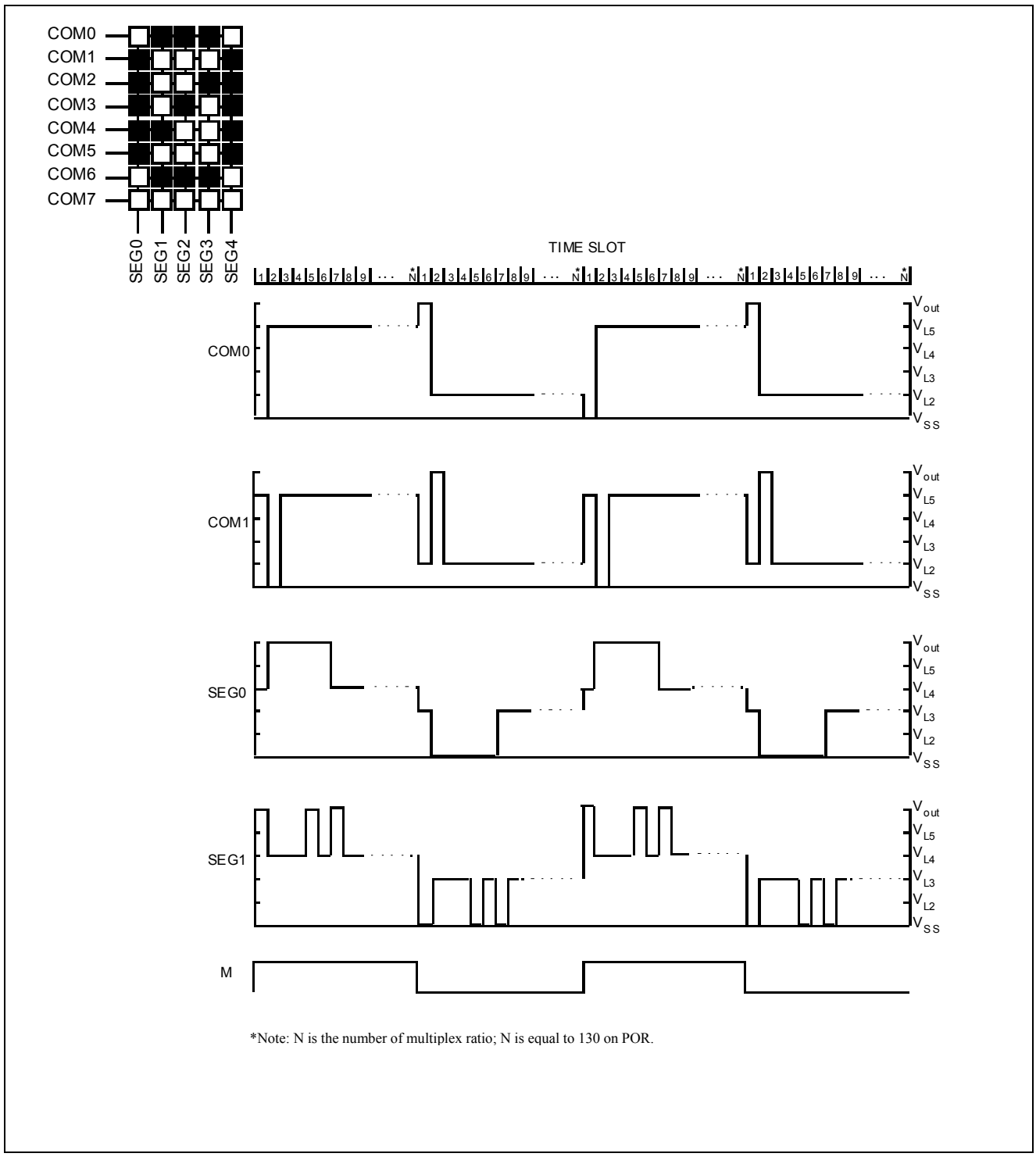
6.31 Level Selector

This block is embedded in the Segment/Common Driver circuits. Level Selector is a control of the display synchronization. Display voltage levels can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

6.32 LCD Panel Driving Waveform

Figure 6-5 is an example of how the Common and Segment drivers may be connected to a LCD panel.

Figure 6-5 - illustration of the segment and common waveform



*Note: N is the number of multiplex ratio; N is equal to 130 on POR.

7 COMMAND TABLE

Table 7-2: COMMAND TABLE (D/$\overline{C}$= 0, R/$\overline{W}$ ($\overline{WR}$) = 0, E=1($\overline{RD}$ = 1) unless specific setting is stated)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	15	0	0	0	1	0	1	0	1	Set Column Address	Set the start column address by $X_5X_4X_3X_2X_1X_0$
1		0	0	X_5	X_4	X_3	X_2	X_1	X_0		Set the end column address by $Y_5Y_4Y_3Y_2Y_1Y_0$
1		0	0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0		Column address = 00000000b (POR) Column address is in a range of 0~32 (0x00~0x20).
0	75	0	1	1	1	0	1	0	1	Set Page Address	Set the start page address by $X_7X_6X_5X_4X_3X_2X_1X_0$
1		X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0		Set the end page address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$
1		Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0		Page address = 00000000b (POR) Page address is in a range of 0~129 (0x00~0x81).
0	BB	1	0	1	1	1	0	1	1	Set COM Output Scan Direction	X_2 X_1 X_0 ROW0…ROW64 ROW65…ROW129 0 0 0 COM0 ->COM64 COM65-> COM129(POR) 0 0 1 COM0->COM64 COM129<-COM65 0 1 0 COM64<-COM0 COM65->COM129 0 1 1 COM64<-COM0 COM129<-COM65
1		*	*	*	*	*	X_2	X_1	X_0		

<table>
<tr><th>D/C</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>BC</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Set Data Output Scan Direction and Grayscale</td><td>a) Normal or Reverse page/column/RAM access/scan directions
P_{10} = 0: set page address to normal display (POR)
P_{10} = 1: set page address to inverse display
P_{11} = 0: set column address to normal rotation (POR)
P_{11} = 1: set column address to inverse rotation
P_{12} = 0: set scan direction to column scan(POR)
P_{12} = 1: set scan direction to page scan
P_{13} = 0: set normal scan direction (POR)
P_{13} = 1: set inverse scan direction

b) Gray-scale setting
X = Light gray PWM count (POR 5 counts)
Y = Dark gray PWM count (POR 10 counts)
$P_{22}P_{21}P_{20}$ = X -1 (POR 100)
$P_{25}P_{24}P_{23}$ = Y - X - 1 (POR 100)
Remark: Y-X≤8

* Remarks: The PWM count for White and Black are 0 and 15 respectively.

P_{30} = 0: PWM (POR)

P_{34} = 0:

<table><tr><td>White</td><td>Light Gray</td><td>Dark Gray</td><td>Black</td></tr><tr><td>0%</td><td>33%</td><td>66%</td><td>100%</td></tr></table>
P_{34} = 1:

<table><tr><td>White</td><td>Light Gray</td><td>Dark Gray</td><td>Black</td></tr><tr><td>0%</td><td>X/15</td><td>Y/15</td><td>100%</td></tr></table>
P_{30} = 1: FRC

P_{31} = 0: 3-frame FRC (POR)

<table><tr><td>White</td><td>Light Gray</td><td>Dark Gray</td><td>Black</td></tr><tr><td>0%</td><td>33%</td><td>66%,</td><td>100%</td></tr></table>
P_{31} = 1: 4-frame FRC

<table><tr><td>P_{33} P_{32}</td><td>White</td><td>Light Gray</td><td>Dark Gray</td><td>Black</td></tr><tr><td>00(POR)</td><td>0%</td><td>25%</td><td>75%,</td><td>100%</td></tr><tr><td>01</td><td>0%</td><td>50%</td><td>75%</td><td>100%</td></tr><tr><td>10</td><td>0%</td><td>25%</td><td>50%</td><td>100%</td></tr><tr><td>11</td><td colspan="4">Reserved</td></tr></table></td></tr>
</table>

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1 1	CA	1 0 * 0	1 0 * 0	0 0 Y_5 0	0 0 Y_4 0	1 0 Y_3 0	0 0 Y_2 0	1 0 Y_1 0	0 0 Y_0 0	Set Display Control	Driver duty selection Select driver duty from 1/16 to 1/128. As $Y_5Y_4Y_3Y_2Y_1Y_0$ is increased from 000011b to 011111b, the number of display lines, N is increased at the same rating. To specify the $Y_5Y_4Y_3Y_2Y_1Y_0$ = (N/4)-1 where 1/N is the driver duty. $Y_5Y_4Y_3Y_2Y_1Y_0$ = 100000b for 1/130 duty.
0 1 1 1 1	AA	1 X_7 Y_7 Z_7 *	0 X_6 Y_6 Z_6 *	1 X_5 Y_5 Z_5 *	0 X_4 Y_4 Z_4 *	1 X_3 Y_3 Z_3 *	0 X_2 Y_2 Z_2 *	1 X_1 Y_1 Z_1 P_{41}	0 X_0 Y_0 Z_0 P_{40}	Set Area Scroll	a) Top Block Address $X_7X_6X_5X_4X_3X_2X_1X_0$ is used to specify the row address at the top of the scrolling area. Top row address = 00000000b (POR) b) Bottom Block Address $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ is used to specify the row address at the bottom of the scrolling area. Bottom row address = 00000000b (POR) c) Number of specified Blocks The number of specified blocks = Number of (Top fixed area + Scroll area) blocks –1. If bottom scroll or whole screen scroll mode is chosen, the number of specified blocks is set to $Z_7Z_6Z_5Z_4Z_3Z_2Z_1Z_0$ Number of specified blocks = 00000000b (POR) d) Area Scroll Mode There are four types of area scroll. P_{41} P_{40} Types of Area Scroll 0 0 Center Screen Scroll 0 1 Top Screen Scroll 1 0 Bottom Screen Scroll 1 1 Whole Screen Scroll Type of area scroll = Whole Screen Scroll (POR)
0 1	AB	1 X_7	0 X_6	1 X_5	0 X_4	1 X_3	0 X_2	1 X_1	1 X_0	Set Scroll Start	$X_5X_4X_3X_2X_1X_0$ specify the start row address of area scrolling. Start block address = 00000000b (POR)
0 1	20	0 *	0 *	1 *	0 X_4	0 X_3	0 X_2	0 X_1	0 X_0	Set Power Control Register	X_0=0: turns off the reference voltage generator (POR) X_0=1: turns on the reference voltage generator X_1=0: turns off the internal regulator and voltage follower (POR) X_1=1: turns on the internal regulator and voltage follower Select booster level X_4 X_3 X_2 Boost level 0 0 0 4X 0 0 1 5X 0 1 0 6X (POR) 0 1 1 7X

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	81	1 * *	0 * *	0 X_5 *	0 X_4 *	0 X_3 *	0 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Contrast Level & Internal Regulator Resistor Ratio	a) Select contrast level from 64 contrast steps Contrast increases as $X_5X_4X_3X_2X_1X_0$ is increased from 000000b to 111111b. $X_5X_4X_3X_2X_1X_0$ = 100000b (POR) b) The internal regulator gain (1+R2/R1) V_{OUT} increases as $Y_2Y_1Y_0$ is increased from 000b to 111b. The factor, 1+R2/R1, is given by: $Y_2Y_1Y_0$ = 000: 3.38 (POR) $Y_2Y_1Y_0$ = 001: 4.41 $Y_2Y_1Y_0$ = 010: 5.44 $Y_2Y_1Y_0$ = 011: 6.47 $Y_2Y_1Y_0$ = 100: 7.50 $Y_2Y_1Y_0$ = 101: 8.52 $Y_2Y_1Y_0$ = 110: 9.55 $Y_2Y_1Y_0$ = 111: 10.58
0 1 1	A8	1 0 X_7	0 0 X_6	1 0 X_5	0 0 X_4	1 0 X_3	0 0 X_2	0 0 X_1	0 0 X_0	Enter partial Display	$X_7X_6X_5X_4X_3X_2X_1X_0$: End COM Address = 00000000b (POR)
0	A9	1	0	1	0	1	0	0	1	Exit partial Display	Exit the "partial display mode" by executing the command 10101001b (POR)
0	AE - AF	1	0	1	0	1	1	1	X_0	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
0	94 - 95	1	0	0	1	0	1	0	X0	Enter/Exit sleep mode	X0=0: exit the sleep mode. X0=1: enter sleep mode. (POR)
0	D1 – D2	1	1	0	1	0	0	X_1	X_0	Enable/disable internal oscillator	X_1 X_0 Internal oscillator status 0 1 ON 1 0 OFF (POR)
0 1	82	1 *	0 *	0 *	0 *	0 *	0 *	1 X_1	0 X_0	Set temperature compensation coefficient	VOUT average temperature gradients X_1 X_0 Average Temperature Gradient [%/oC] 0 0 -0.01 (POR) 0 1 -0.06
0	25	0	0	1	0	0	1	0	1	NOP	Command result in No Operation The command should be issued after the execution of the Status Read command
0 1	5C	0 Y_{71}	1 Y_{61}	0 Y_{51}	1 Y_{41}	1 Y_{31}	1 Y_{21}	0 Y_{11}	0 Y_{01}	Write display data	Enter the "write display data mode" by executing the command 01011100b. The following byte is used to specify the data byte to be written to the GDDRAM directly. The D/C bit should be stated at logic "1" during the display data is written to the GDDRAM.

Remark: "" denote DON'T CARE* bit

Table 8-3: Extended command table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0/1	FB	1 L_0	1 0	1 0	1 0	1 B_3	0 B_2	1 B_1	1 B_0	Set biasing ratio & Command lock/unlock	Allow user to set bias from 1/ 4 to 1/13 $B_3B_2B_1B_0$ Bias ratio 1 0 0 1 1/4 bias 1 0 0 0 1/5 bias 0 1 1 1 1/6 bias 0 1 1 0 1/7 bias 0 1 0 1 1/8 bias 0 1 0 0 1/9 bias 0 0 1 1 1/10 bias 0 0 1 0 1/11 bias 0 0 0 1 1/12 bias 0 0 0 0 1/13 bias (POR) L_0 Lock and unlock Cmd 0 unlock (POR) 1 lock and no more cmd/data is written to driver The 2nd byte is sent as Cmd if L_0 is set to 1
0 1 1	F2	1 0 X_0	1 1 N_6	1 F_4 N_5	1 F_3 N_4	0 F_2 N_3	0 F_1 N_2	1 F_0 N_1	0 0 N_0	Set Frame frequency and N-line Inversion	This command uses to change the frame frequency; set the N-line inversion and N-line inversion mode X_0 = 1 (POR) X_0 = 0 $F_4F_3F_2F_1F_0$ 00000 : 56.4 Hz (POR) 64Hz 00111 : +10.1% +11.8% 01000 : +10.7% +15.2% 01001 : +12.5% +15.2% 01010 : +14.1% +20.6% 01011 : +16.1% +20.6% 01100 : +17.4% +25.9% 01101 : +19.5% +25.9% 01110 : +21.4% +32.9% 01111 : +23.7% +32.9% 10000 : +24.6% +37.4% 10001 : +27.1% +37.4% 10010 : +29.2% +46.0% 10011 : +31.8% +46.0% 10100 : +33.6% +54.6% 10101 : +36.5% +54.6% 10110 : +39.0% +66.9% 10111 : +42.2% +66.9% 11000 : +43.2% +75.8% 11001 : +46.6% +75.8% 11010 : +49.7% +94.0% Remark: The frame frequency is typical value for 130mux and PWM mode. The second byte data $N_5N_4N_3N_2N_1N_0$ sets the n-line inversion register from 2 to 64 lines to reduce display crosstalk. Register values from 000001b to 111111b are mapped to 2 lines to 64 lines respectively. Value 00000b disables the N-line inversion. 010000 is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux should NOT be a multiple of the lines of inversion (n). N_6 0 – reset n-line counter per frame (POR) 1 – will not reset n-line counter per frame

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	F6	1 Y_2 0	1 Y_1 0	1 0 0	1 X_4 0	0 X_3 0	1 X_2 1	1 X_1 1	0 X_0 0	Dual OTP setting	This command set the offset value of contrast for the first time and the second time OTP $X_4X_3X_2X_1X_0$ (Emulate/Program) 00000 : original contrast (+ 0 fine step/ -1 fine step) 00001 : original contrast (+ 1 fine step/ -2 fine steps) 00010 : original contrast (+ 2 fine steps/ -3 fine steps) 00011 : original contrast (+ 3 fine steps/ -4 fine steps) 00100 : original contrast (+ 4 fine steps/ -5 fine steps) 00101 : original contrast (+ 5 fine steps/ -6 fine steps) 00110 : original contrast (+ 6 fine steps/ -7 fine steps) 00111 : original contrast (+ 7 fine steps/ -8 fine steps) 01000 : original contrast (+ 8 fine steps/ -9 fine steps) 01001 : original contrast (+ 9 fine steps/ -10 fine steps) 01010 : original contrast (+10 fine steps/-11 fine steps) 01011 : original contrast (+11 fine steps/-12 fine steps) 01100 : original contrast (+12 fine steps/-13 fine steps) 01101 : original contrast (+13 fine steps/-14 fine steps) 01110 : original contrast (+14 fine steps/-15 fine steps) 01111 : original contrast (+15 fine steps/-16 fine steps) 10000 : original contrast (–16 fine steps/+15 fine steps) 10001 : original contrast (- 15 fine steps/+14 fine steps) 10010 : original contrast (- 14 fine steps/+13 fine steps) 10011 : original contrast (- 13 fine steps/+12 fine steps) 10100 : original contrast (- 12 fine steps/+11 fine steps) 10101 : original contrast (- 11 fine steps/+10 fine steps) 10110 : original contrast (- 10 fine steps/+ 9 fine steps) 10111 : original contrast (- 9 fine steps/+ 8 fine steps) 11000 : original contrast (- 8 fine steps/+ 7 fine steps) 11001 : original contrast (- 7 fine steps/+ 6 fine steps) 11010 : original contrast (- 6 fine steps/+ 5 fine steps) 11011 : original contrast (- 5 fine steps/+ 4 fine steps) 11100 : original contrast (- 4 fine steps/+ 3 fine steps) 11101 : original contrast (- 3 fine steps/+ 2 fine steps) 11110 : original contrast (- 2 fine steps/+ 1 fine step) 11111 : original contrast (- 1 fine step/+ 0 fine step) Y_1 = 0: 1st Level OTP (POR) Y_1 = 1: 2nd Level OTP Y_2 = 0: Emulate OTP step Y_2 = 1: Enable OTP (POR) Remarks: 2nd level OTP cannot be executed before 1st level OTP. Y_2Y_1 = 00, $X_3X_2X_1X_0$ = 0000: Disable OTP function * Note: 1 contrast step = 2 fine steps
0	F8	1	1	1	1	1	0	0	0	OTP programming	This command starts to program LCD driver with OTP offset value. This command can be executed twice only. Detail of OTP programming procedure on page 36
0 1	44	0 A_7	1 A_6	0 A_5	0 A_4	0 A_3	1 A_2	0 A_1	0 A_0	Set 1st Com Line	Set 1st Com-line command. Byte A specifies the number of scroll lines. $A_7A_6A_5A_4A_3A_2A_1A_0$ = 00000000 (POR) Byte A is ranging from 0 to 129

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	F7	1	1	1	1	0	1	1	1	Grayscale or mono mode selection	Y_0 = 0 : Grayscale mode (POR)
1		0	0	0	0	0	0	0	0		Y_0 = 1 : Mono mode
1		0	0	0	0	1	1	1	0		
1		0	Y_0	0	0	0	0	0	1		

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	5D	0	1	0	1	1	1	0	1	Read display data	Enter the "read display data mode" by executing the command 01011101b. The next byte is a dummy data. The GDDRAM data will be read form the second byte. The GDDRAM column address pointer will be increased by one automatically after each 2-bytes data read.
1		Y_{71}	Y_{61}	Y_{51}	Y_{41}	Y_{31}	Y_{21}	Y_{11}	Y_{01}		
0	F3	1	1	1	1	0	0	1	1	Bias current, booster frequency & OTP status read selection	This command selects the bias current for VL5, VL4, VL3 and VL2, the booster frequency and the 1st and 2nd OTP status read. A_2 A_1 A_0: bias current for VL3 and VL2 A_6 A_5 A_4: bias current for VL5 and VL4 000 : 1.0 x I_{ref} 001 : 3.5 x I_{ref} 010 : 6.0 x I_{ref} (POR) 011 : 8.5 x I_{ref} 100 : 11.0 x I_{ref} 101 : 13.5 x I_{ref} 110 : 17.0 x I_{ref} 111 : 18.5 x I_{ref} X_1X_0 00 : Fosc/2 (POR) 01 : Fosc/4 10 : Fosc/8 11 : Fosc/16 $Y_2Y_1Y_0$ = 000: Read 1st Level OTP (POR) $Y_2Y_1Y_0$ = 111: Read 2nd Level OTP where I_{ref} is a constant
1		1	A_6	A_5	A_4	0	A_2	A_1	A_0		
1	15	0	0	0	1	0	1	0	1		
1	00	0	0	0	0	0	0	0	0		
1		1	0	0	Y_2	Y_1	Y_0	X_1	X_0		
0	F9	1	1	1	1	1	0	0	1	Read back dual OTP value, SSL module identity & OTP register status	A_4 A_3 A_2 A_1 A_0 = OTP value
0		*	*	*	A_4	A_3	A_2	A_1	A_0		

Table 8-4: Read Command Table

Note: Command patterns other than that given in Command Table are prohibited. Otherwise, unexpected result will occur.
Remark: "" denote DON'T CARE* bit

To read data from the GDDRAM, 5Dhex command should be executed then input High to $R/\overline{W}$ ($\overline{WR}$) pin and $D/\overline{C}$ pin for 6800-series parallel mode. Low to E($\overline{RD}$) pin and High to $D/\overline{C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be

increased by one automatically after each data read in 4 pixels per 8 bit in GS mode OR 8 pixels per 8 bit in BW mode. Also, a dummy read is required before the first data is read. See Figure 6-1.

To write data to the GDDRAM, input Low to $R/\overline{W}$ ($\overline{WR}$) pin and High to E($\overline{RD}$) pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write in 4 pixels per 8 bit in GS mode OR 8 pixels per 8 bit in BW mode. The address will be reset to 0 in next data read/write operation is executed when it is 32.

8 COMMAND DESCRIPTIONS

8.1 Set Column Address (15 H)

This command specifies the 6-bit column address of the display data RAM. The start and the end column address are specified by this command. The driver supports up to 130 columns. As the addresses are incremented from the start column to the end column in the column direction scan, the page address is incremented by 1. The column address is then returned to the start column. The column address will be increased by each data access after it is preset by the MCU. Start column < End column must be maintained.

8.2 Set Page Address (75 H)

This command enters the page address from 0 to 127 to the RAM page register for read/write operations. The driver supports up to 130 lines. All in all, there are 130 pages. As the addresses are incremented from the start page to the end page in the page direction scan, the column address is incremented by 1. The page address is then returned to the start page. Start page < End page must be maintained.

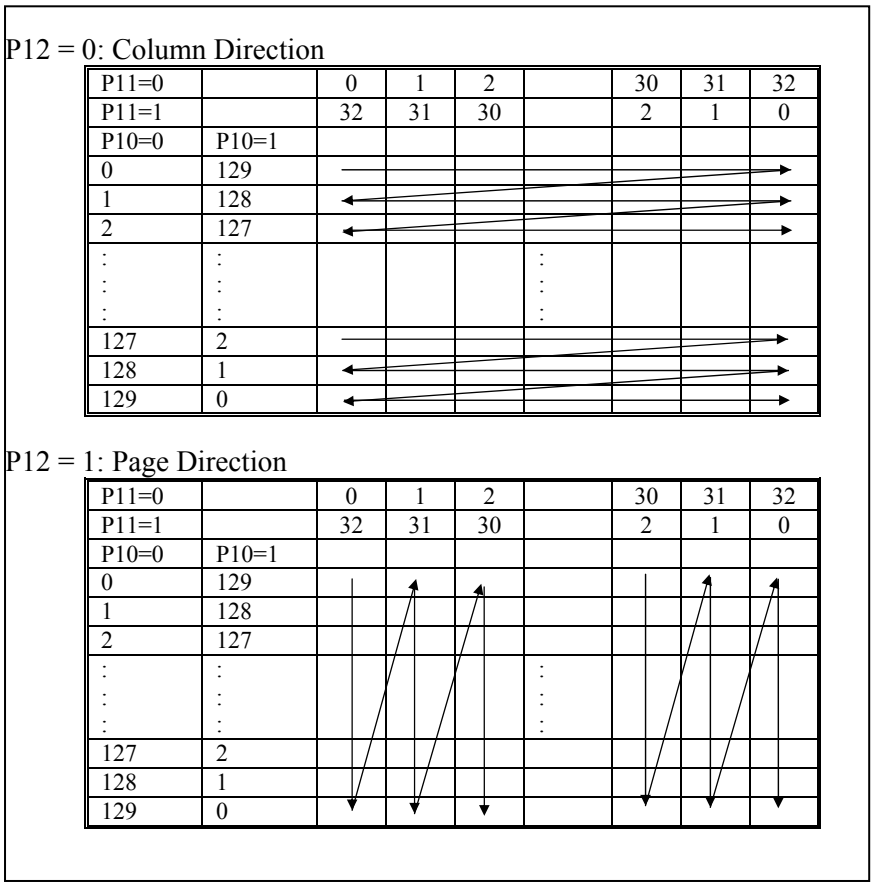
8.3 Set COM Output Scan Direction (BB H)

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. Please refer to the on Page 23 for detail mapping. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

8.4 Set Data Output Scan Direction (BC H)

This command sets the DDRAM such that the MPU operates the display data in the internal RAM.
The Data Scan direction can be set to either normal or inverse display page and column address scan direction. The column and the page direction are illustrated in the following figure.

Figure 8-6: Column and page scan direction



8.5 Set Grayscale (BC H)

GDDRAM data	Normal Display(0xA6)	Inverse display(0xA7)
00	White	Black
01	Light Gray	Dark Gray
10	Dark Gray	Light Gray
11	Black	White

1. Using PWM (P_{30}=0)

There are total 15 counts for PWM used to generate different grayscales. The percentage of black can be calculated by number of counts divided by 15. There are two kinds of PWM settings, customized and default by setting P_{34} to 1 and 0 respectively.

Set P_{34}=1 for customized PWM.

Customer can define the number of PWM counts for Light Gray and Dark Gray. White and Black, by default, are 0 and 15 counts respectively.

Let X and Y be the number of counts for Light Gray and Dark Gray, where Y-X≤8,

P_{22} P_{21} P_{20}=X-1
P_{25} P_{24} P_{23}=Y-X-1

Example:

X=3 Y=11
P_{22} P_{21} P_{20} = 010
P_{25} P_{24} P_{23} = 111

The grayscales setting will be:

	Number of count	Percentage	Color
White	0	0%	
Light Gray	3	20%	
Dark Gray	11	73%	
Black	15	100%	

Set P_{34}=0 for default PWM. The grayscale settings will be:

	Number of count	Percentage	Color
White	0	0%	
Light Gray	5	33%	
Dark Gray	10	66%	
Black	15	100%	

2. Using FRC (P_{30}=1)

There are two kinds of FRC, 3-frame and 4-frame. The number of PWM counts in a frame is either 0 or 15. The percentage of black can be calculated by the number of frame with full PWM counts divided by either 3 or 4 (for 3-frame and 4-frame FRC respectively).

Set P_{31}=0 for 3-frame FRC.

	Frame 1	Frame 2	Frame 3	Percentage	Color
White	0	0	0	0%	
Light Gray	15	0	0	33%	
Dark Gray	15	15	0	66%	
Black	15	15	15	100%	

Set P_{31}=1 for 4-frame FRC.

When $P_{33}P_{32}$=00,

	Frame 1	Frame 2	Frame 3	Frame 4	Percentage	Color
White	0	0	0	0	0%	
Light Gray	15	0	0	0	25%	
Dark Gray	15	15	15	0	75%	
Black	15	15	15	15	100%	

When $P_{33}P_{32}$=01,

	Frame 1	Frame 2	Frame 3	Frame 4	Percentage	Color
White	0	0	0	0	0%	
Light Gray	15	0	15	0	50%	
Dark Gray	15	15	15	0	75%	
Black	15	15	15	15	100%	

When $P_{33}P_{32}$=10,

	Frame 1	Frame 2	Frame 3	Frame 4	Percentage	Color
White	0	0	0	0	0%	
Light Gray	15	0	0	0	25%	
Dark Gray	15	0	15	0	50%	
Black	15	15	15	15	100%	

8.6 Set Display Control (CA H)

This command is used to select the duty ratio of the IC. All available driving duty can be selected using this command. The driving duty can be changed from 1/16 to 1/128 or 1/130.

8.7 Set Area Scroll (AA H)

This command specifies the portion of screen for scrolling. The command sets the starting block address, finishing block address, number of specific blocks and the area scroll mode of the area scrolling. Please be noted that the starting block address should be smaller than the finishing block address.
The block address increment direction is started at 0^{th} block such that the GDDRAM address corresponds to the top of the fixed area. Similarly, the block address decrement direction is started at the 32^{nd} block such that the GDDRAM address corresponds to the bottom fixed area. The remaining block address excluding the top and the bottom fixed areas are assigned to the scroll plus the background areas.
The set area scroll function is divided into four parts.

Part I -Specify the top block address of the scroll + the background areas. Specify the 0^{th} block for the top screen scroll or the whole screen scroll. The scroll start block address is also set at this top block address until the scroll start set command is executed.

Part II – Specify the bottom address of the scroll + background areas. Specify the 32^{nd} block for the bottom or the whole screen scroll.

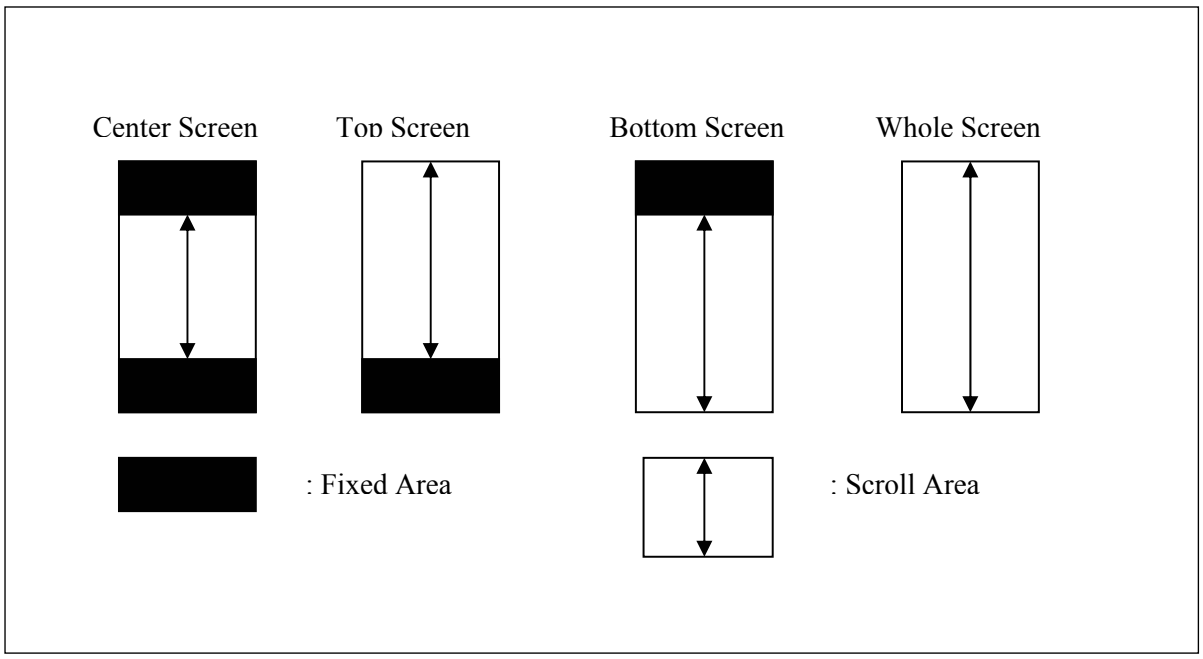
Part III – Specify number of scrolled blocks = number of (Top fixed area + scroll area) blocks –1. When the bottom scroll or whole screen scroll is chosen, the resulted value is identical to the value stated in part II.

Part IV - Specify the area scroll type. Altogether there are four types of area scroll. Please refer to Table 8-5 for detail.

Table 8-5: Area scrolling selection modes

P41	P40	Types of Area Scroll
0	0	Center Screen Scroll
0	1	Top Screen Scroll
1	0	Bottom Screen Scroll
1	1	Whole Screen Scroll

Figure 8-7: Area scrolling selection modes



The area scroll function is executed by prompt in the set area scroll command following by changing the start block address by the set scroll start command. Figure 8-7Figure illustrates the operation model of the scrolling function.

Example: In the Center screen scroll of 1/96 duty (display range: 96 lines = 24 blocks)

Description	Command	Data
- Set Area Scroll	AA H	
- 8 lines (block 0 to block 1) is specified for the top fixed area		
Top block address = Number of lines in top fixed area / 4		
= 8 / 4		
= 2		02 H
- 8 lines (block 30 to block 31) are specified for the bottom fixed area		
Bottom block address = 31 – (number of lines in bottom fixed area / 4)		
= 31 – (8 / 4)		
= 31 – 2 = 29		1D H
- 96 lines (block 2 to block 25) are specified the scroll area		
Number of specified block		
= Top block address + (number of lines in scroll area / 4) – 1		
= 2 + (96 / 4) –1		
= 2 + 24 – 1 = 25		19 H
- 16 lines (block 26 to block 29) are specified the background areas		
- Set area scroll mode – Center screen mode		00 H
- Set Scroll start (Scroll range form 02H ~ 29H)	AB H	
		02 H

Figure 8-8: GDDRAM updates for area scrolling

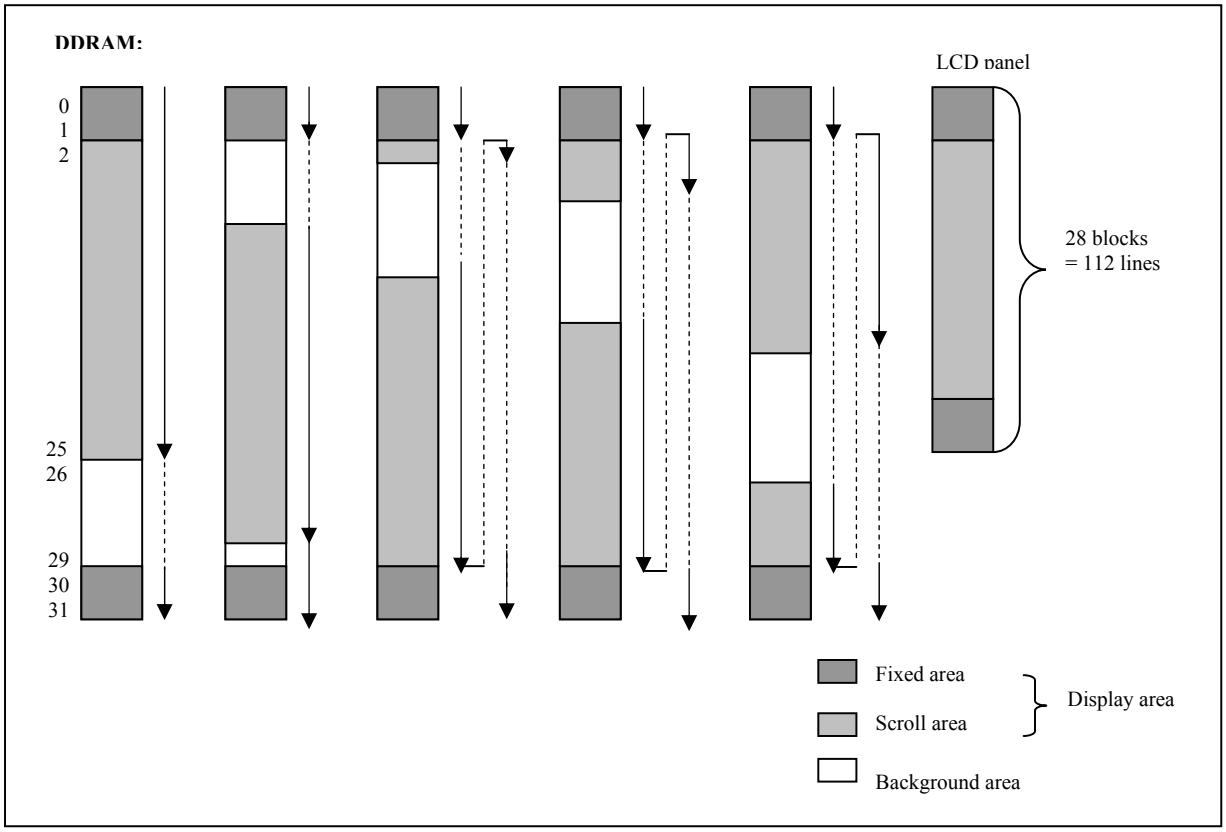
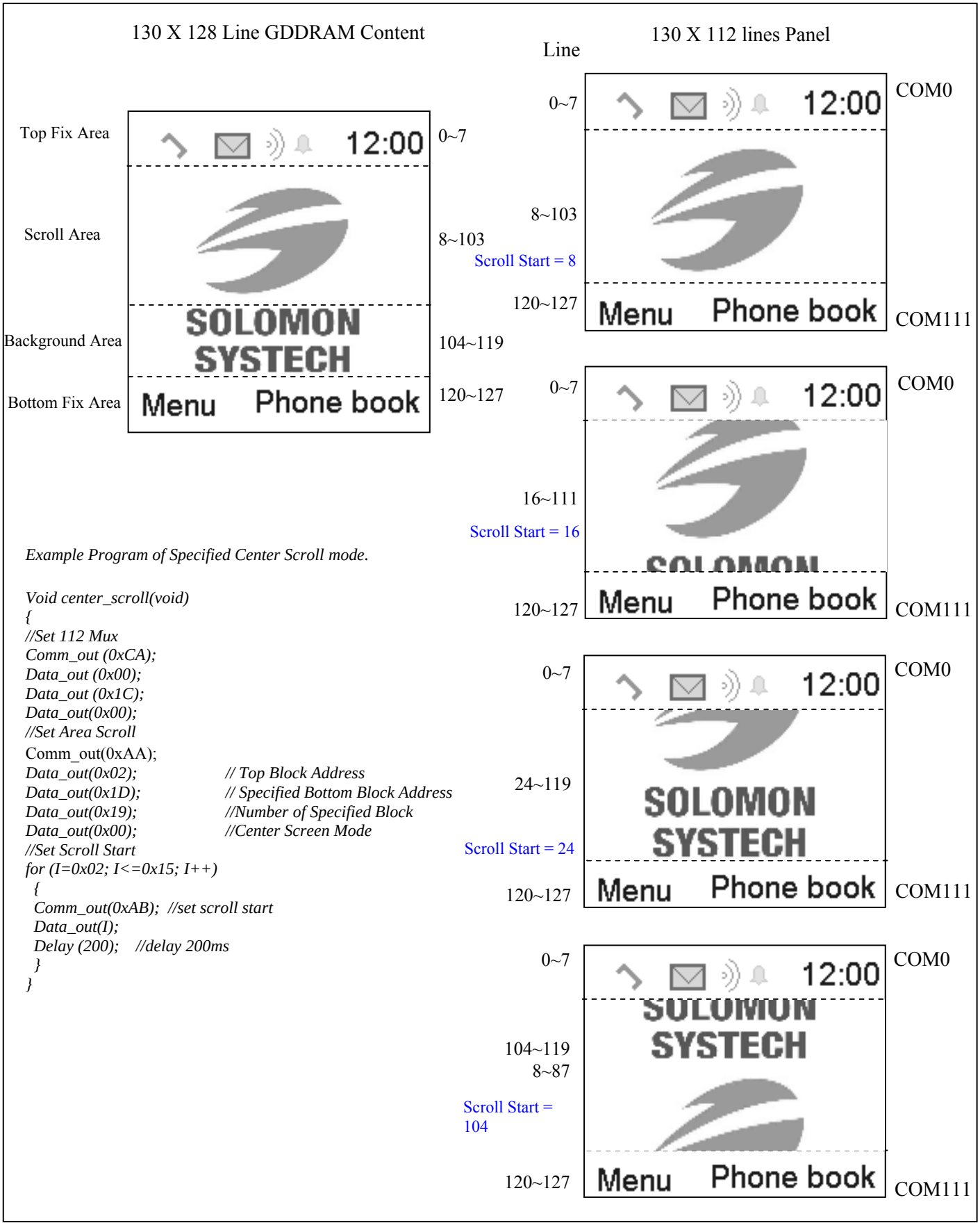


Figure 8-9: Example of center scroll mode



Example Program of Specified Center Scroll mode.

```
Void center_scroll(void)
{
//Set 112 Mux
Comm_out (0xCA);
Data_out (0x00);
Data_out (0x1C);
Data_out(0x00);
//Set Area Scroll
Comm_out(0xAA);
Data_out(0x02);          // Top Block Address
Data_out(0x1D);          // Specified Bottom Block Address
Data_out(0x19);          //Number of Specified Block
Data_out(0x00);          //Center Screen Mode
//Set Scroll Start
for (I=0x02; I<=0x15; I++)
  {
  Comm_out(0xAB);  //set scroll start
  Data_out(I);
  Delay (200);    //delay 200ms
  }
}
```

8.8 Set Scroll Start (AB H)

This command specifies the starting block address of the area scrolling and then executes the area scroll by changing the start block address dynamically. Start block < End block must be maintained. Please be noted that the set scroll start command should be executed after the set area scroll command.

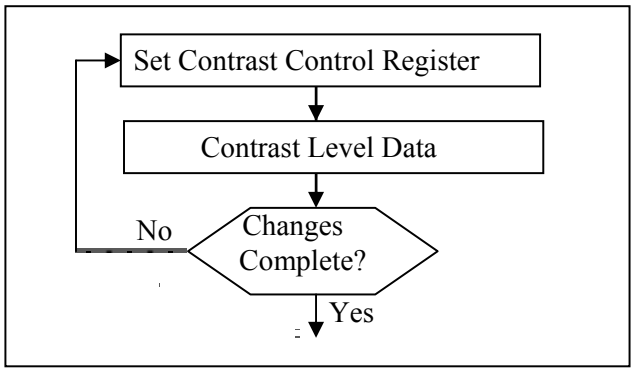
8.9 Set Power Control Register (20 H)

This command turns on/off the various power circuits associated with the chip. There are three power sub-circuits (reference voltage generator, internal regulator and voltage follower) could be turned on/off by this command. In addition, the configuration of the internal primary booster (4X/5X/6X/7X) can be selected by this command.

8.10 Set Contrast Level and Internal Regulator Resistor Ratio (IR) (81 H)

This command adjusts the contrast of the LCD panel by changing the LCD driving voltage, VOUT, provided by the On-Chip power circuits. VOUT is set with 64 steps (6-bit) in the contrast control register by a set of compound commands. Please refer to the Figure 8-10 for the contrast control process flow diagram.

Figure 8-10: Contrast Control Flow Set Segment Re-map

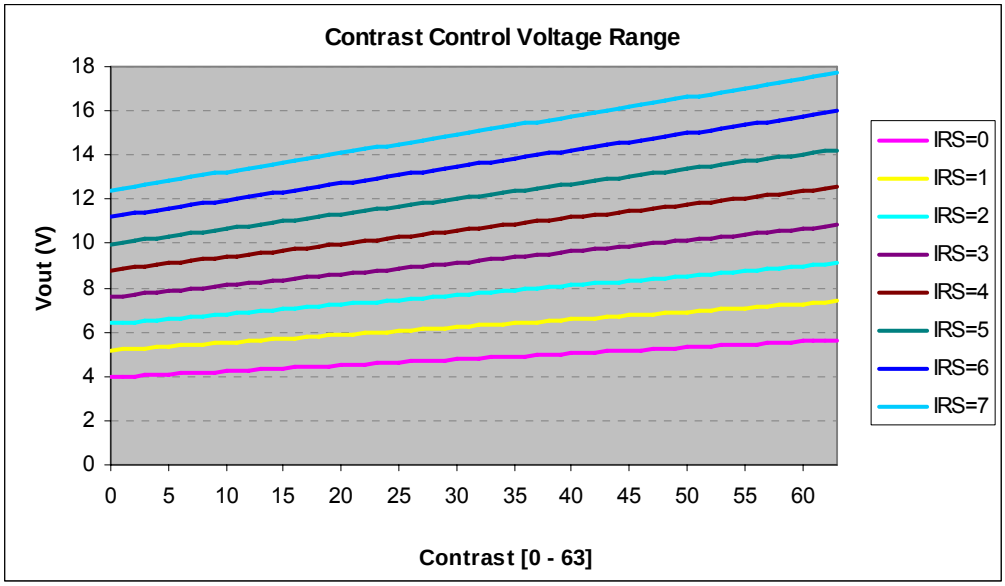


This command also sets the feedback gain of the internal regulator. There are altogether 8 internal regulator gains, which are used for the adjustment of V_{OUT} level. This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network. The Contrast Control Voltage Range curves is referred to the following formula:

$$V_{out} = [\ 1 + R_2 / R_1] * V_{con}$$
$$V_{con} = [1 + \alpha / 148\ ] * V_{ref}$$

where Vref = 1.173, PTC = 0

Figure 8-11: Contrast Control Voltage Range Curve at Room temp with PTC = 0



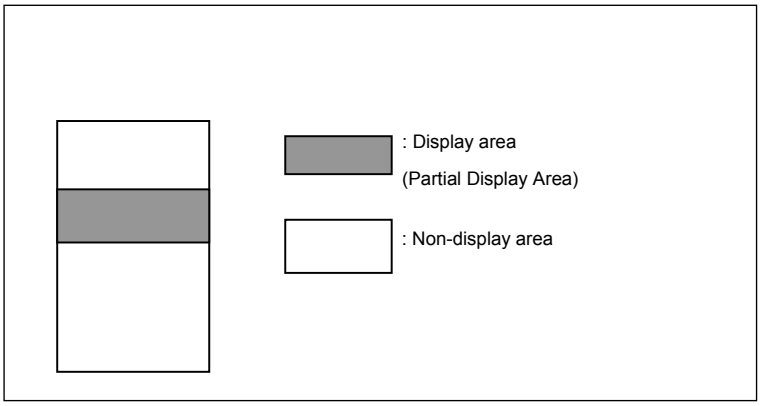
8.11 Set Normal/Inverse Display (A6/A7 H)

This command turns the display to be either normal (A6 H) or inverse (A7). In normal display mode, a RAM data of 1 indicates an illumination on the corresponding pixel in the normal white panel. In inverse display mode, a RAM data of 0 will turn on the pixel.

8.12 Enter Partial Display (A8 H)

This command and the following parameters specify the display area of the partial display mode. The following figure shows the display and non-display area when the partial display mode is executed.

Figure 8-12: Partial display mode



8.13 Exit Partial Display (A9 H)

This command exits the partial display mode.

8.14 Set Display On/Off (AF/AE H)

This command is used to turn the display on (AF H) or off (AE H). When display off is issued with entire display is on, power save mode will be entered.

8.15 Enter/Exit sleep mode (95/94 H)

This command enters (95 H) or exit (94 H) the sleep mode.

8.16 Enable/Disable the internal oscillator (D1/D2 H)

This command enables (D1 H) or disables (D2 H) the internal oscillator. The internal oscillator is turned off after reset.

8.17 Set Temperature compensation coefficient (82 H)

This command sets the average temperature gradients. Two sets of average temperature gradients can be selected for VOUT voltage. Please refer to the command table for detail description of the average temperature gradients. The default value of the VOUT temperature gradient is –0.01 %/^{0}C.

8.18 NOP (25 H)

A command causing the chip takes No Operation.

8.19 Write display data mode (5C H)

This command is used to execute the write display data mode. The display data byte is directly written to the GDDRAM. Please be noted that the $D/\overline{C}$ signal should be set to high during the display data is written to the GDDRAM.

8.20 Set biasing ratio (FB H)

This command selects a suitable bias ratio (1/4 to 1/13) required for driving the particular LCD panel in use. No any command or data can be written to driver when lock command is enabled.

8.21 Set Frame Frequency (F2 H)

This command specifies the frame frequency so as to minimize the flickering due to the ac main frequency.

8.22 Set N-line inversion (F2 H)

Number of line inversion is set by this command for reducing crosstalk noise. 2 to 64-line inversion operations could be selected. At POR, this operation is set to 10000b (17 lines). It should be noted that the total number of mux should NOT be a multiple of the inversion number (n). Or else, some lines will not change their polarity during frame change. The n-line counter can be set such that it will be reset per display frame (POR).

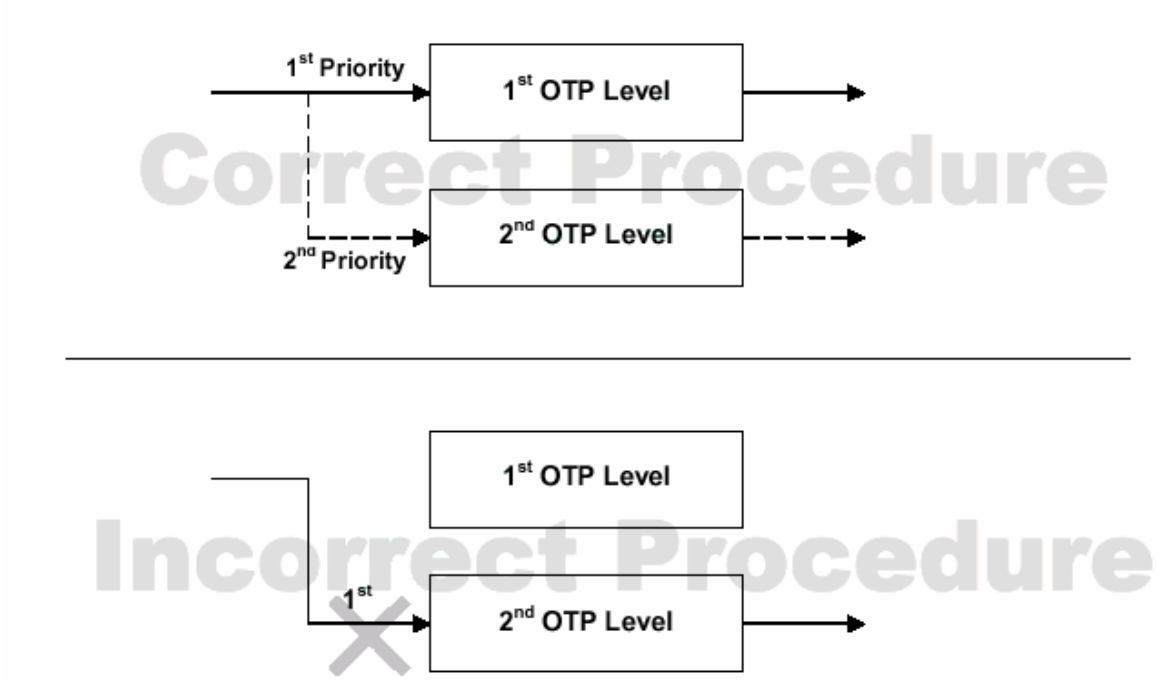
8.23 OTP setting (F6 H)

Vout of the STN driver should be finely adjusted to cope with the characteristics of different LCD panels. The magnitude of Vout affects the contrast level of final LCD module. OTP provides a channel to modify the magnitude of Vout at module level to achieve the optimal contrast level on every LCD module. During OTP process, a high voltage source is applied to OTP cell through Vout pin to set the voltage level permanently.

SSD1848 provides a unique feature, Dual Level OTP, to ensure the best contrast level is obtainable in every single product. For instance, module-manufacturers can trigger the first level OTP to obtain the optimal contrast level in a lot of STN module, while the second level OTP can be optionally launched by the module-user to achieve the best contrast in a single application. It should be reminded that due to the introduction of the dual OTP function, the OTP setting can only be valid if the following procedures are followed.

1. OTP Procedure
In programming the OTP, the 1st OTP level should be programmed first before the used of 2nd OTP level. Otherwise, the OTP programming will become invalid.

Figure 8-13: Correct Procedure for OTP



Step 1. Find OTP offset

(1) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(2) Send original initialization routines
(3) Set and display any test patterns
(4) Disable OTP function (C:0xF6, D: 0x00; D: 0x06)
(5) Adjust the contrast value (C:0xF6, D:0x00~0x1F, D: 0x06) until there is the best visual contrast

Example 1: 1st OTP :

If C:0xF6, D: 0x07, D:0x06 is the best visual contrast
If OTP emulation command is (C:0xF6, D: 0x07, D: 0x06), then
OTP programming command should be (C:0xF6, D: 0x18, D: 0x06)

Example 2: 2nd OTP :

If C:0xF6, D: 0x14, D:0x06 is the best visual contrast
If OTP emulation command is (C:0xF6, D: 0x54, D: 0x06), then
OTP programming command should be (C:0xF6, D: 0x4B, D: 0x06)

Step 2. Check OTP status

(6) Send the Read OTP status command set
    a. C: 0xF3; D: 0xA2; D: 0x15; D: 0x00, D: 100 $X_2X_1X_0$00
    b. C: F9
    c. Read Command status (***$A_4A_3A_2A_1A_0$)
(7) $X_2X_1X_0$ = 000: 1st OTP [4:0] OTP result after burn
    $X_2X_1X_0$ = 111: 2ndOTP [4:0] OTP result after burn
    $A_4A_3A_2A_1A_0$: Programmed value

Step 3. OTP programming

(8) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(9) Enable Oscillator (C: 0xD1) and Exit Sleep Mode (C: 0x94)
(10) Connect an external V_{OUT} by closing the SW1 (see diagram below)
(11) Send OTP programming commands that we find in step 1 and select the 1st or 2nd OTP (refer to the OTP status which can be find in Step 2)
(C: 0xF6, D: 0x00~0x1F, D: 0x06 for 1st OTP / C: 0xF6, D: 0x40~0x5F, D: 0x06 for 2nd OTP)
(12) Send OTP programming command (C: 0xF8)
(13) Wait at least 2 seconds
(14) Disconnect an external V_{OUT} by opening the SW1
(15) Discharge the capacitor C by closing the switch SW2 and wait at least 1 second
(16) Open SW2
(17) Hardware Reset
(18) Verify the result by repeating step 1. (2) – (3)

Figure 8-14: OTP programming circuitry

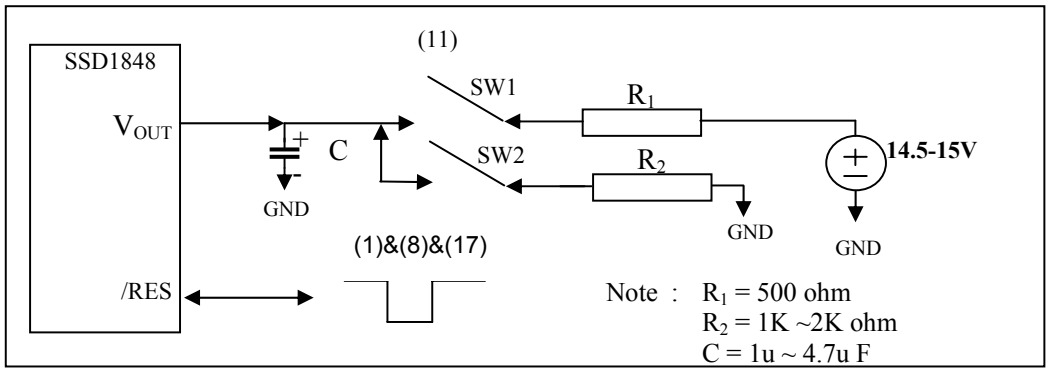
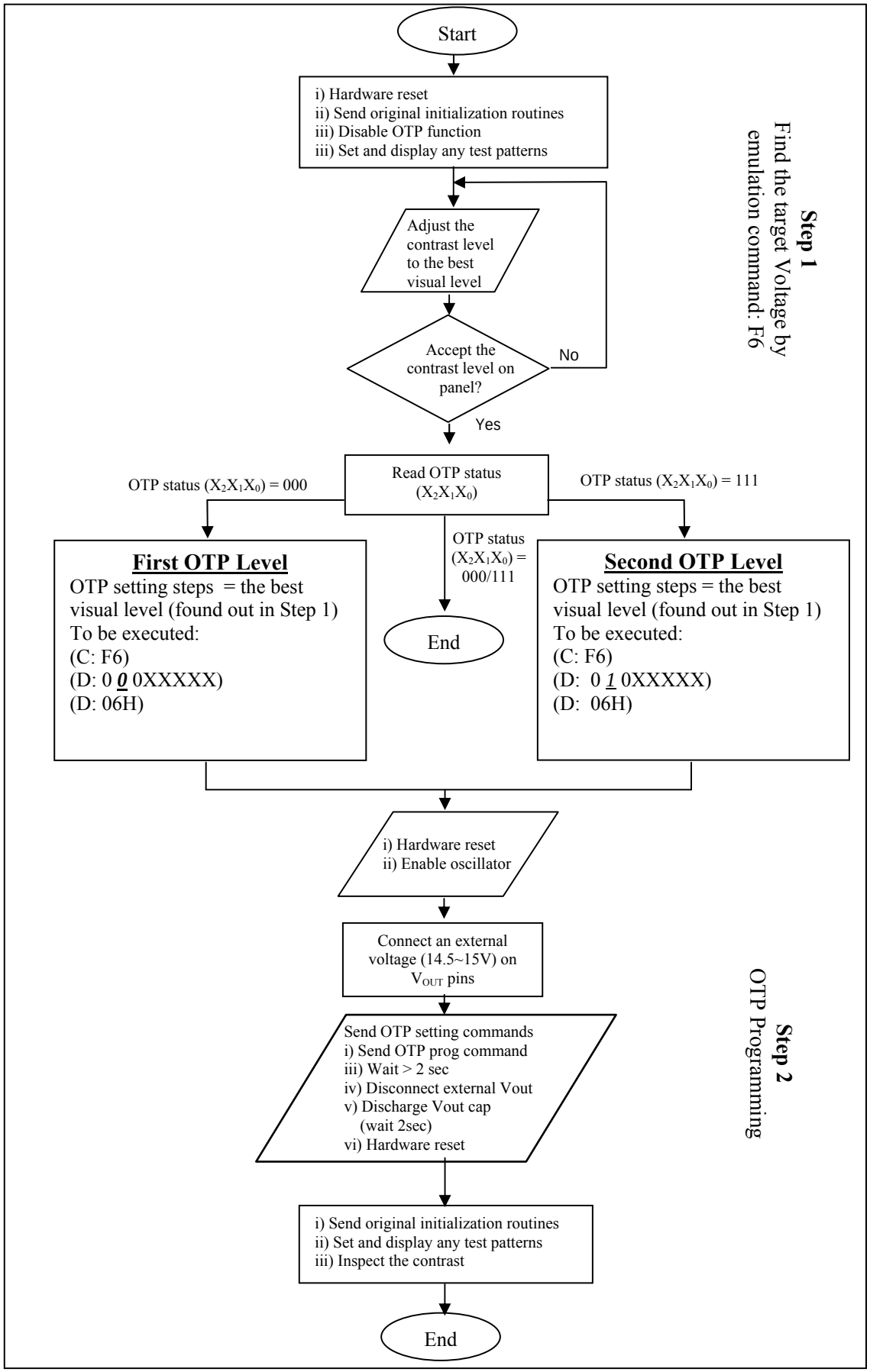


Figure 8-15: Flow chart of OTP programming Procedure



OTP Example program

Step 1 - Find the OTP offset:

1. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
2. COMMAND(0XD1); \\ Enable oscillator;
   COMMAND(0X94); \\ Exit sleep mode;
3. COMMAND(0X20); \\ turn on the reference voltage generator, internal regulator and voltage follower; Select booster l level.
   DATA(0x0B)
4. COMMAND(0XCA) \\ Set Duty ratio
   DATA(0X10) \\ 68Mux ([68 / 4] –1 = 16(decimal) / 10(Hex))
   COMMAND(0XFB) \\ Set Biasing ratio
   DATA(0X26) \\ 1/7
5. COMMAND(0X81) \\ Set target gain and contrast.
   DATA(0X14) \\ contrast = 20
   DATA(0X05) \\ IR5 => gain = 8.52
6. \\ Set target display contents
   COMMAND(0X15) \\ set column address
   DATA(0x00) \\ set start column address at 0
   DATA(0X20) \\ set end column address at 32
   COMMAND(0X75) \\ set page address
   DATA(0X00) \\ set start page address at 0
   DATA(0X81) \\ set end page address at 129
   COMMAND(0X5C) \\ write target content to GDDRAM
   DATA(…)
   COMMAND(0xAF) \\ display on
   COMMAND(0xF6) \\ Disable OTP function and find out the best visual contrast setting
   DATA(0X00 – 1F)
   DATA(0X06)
7. OTP target = C:0xF6, D:0x(00 – 0F), D:0x06 found in previous step. Say, C:0xF6, D:0x12, D:0x06 is the best visual contrast, then OTP programming command is C:0xF6, D:0x0D, D:0x06

Step 2 – Check OTP status:

8. COMMAND(0XF3) \\ Read OTP status command
   DATA(0XA2)
   DATA(0X15)
   DATA(0X00)
   DATA(0X80) \\ 0x80 for 1st OTP, 0x9C for 2nd OTP
   COMMAND(0XF9) \\ Read command
   Read COMMAND \\ D/C=0; R/W=1 for 6800 bus interface OR D/C=0; WR=1; RD=0 for 8080 bus interface
   ***$A_4A_3A_2A_1A_0$ \\ OTP status $A_4A_3A_2A_1A_0$

Step 3 - OTP programming:

9. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
10. COMMAND(0XD1) \\ Enable Oscillator
11. COMMAND(0x94) \\ Exit Sleep Mode
12. Connect a external V_{OUT} (14.5V~15V)
13. COMMAND(0XF6) \\ Set OTP target and program 1st OTP
    DATA (0x0D) \\ 000 $X_4X_3X_2X_1X_0$, where $X_4X_3X_2X_1X_0$ is the inverted OTP contrast steps
    DATA(0x06) \\ Enable the OTP setting
14. COMMAND(0XF8) \\ Send the OTP programming command.
15. Wait at least 2 seconds for programming wait time.
16. Disconnect an external Vout
17. Discharge the Vout's capacitor
18. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin

Verify the result:

19. After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel.

8.24 Set Black & White Mode (F7 H)

This command will set either Grayscale (GS) mode (POR) or Black & White (BW) mode. The GDDRAM data write-in and read-out situation has been shown in Figure 268H8-16. Please note that the original grayscale display data can be resumed when exiting BW mode. The GDDRAM arrangement will follow Figure 6-3 and Figure 6-4 for GS and BW mode respectively.

Figure 8-16: GDDRAM data conversion between Grayscale and Black & White Mode

Grayscale Mode → Black & White Mode → Grayscale Mode

GS data write in	BW data read out	GS data read out
00	0	00
01	0	01
10	1	10
11	1	11

Black & White Mode → Grayscale Mode → Black & White Mode

BW data write in	GS data read out	BW data read out
0	00	0
1	10	1

8.25 OTP Programming (F8 H)

This command initiate OTP program LCD driver with OTP offset value.

8.26 Set 1st Com line (44 H)

This command specifies 1st Com line function. Byte A specifies the first display line which the graphic start to display. At POR, the 1st Com line is set to 00000000b (0 lines).

8.27 Read display data mode (5D H)

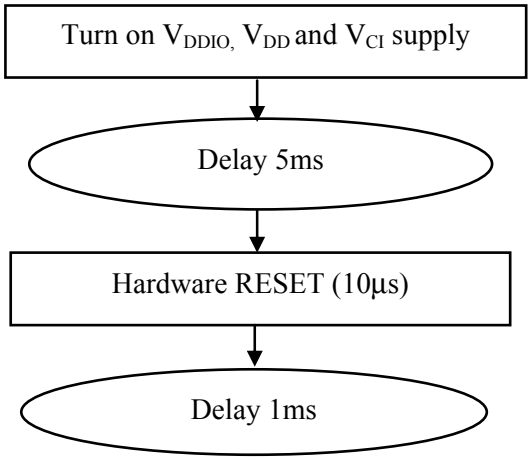
This command is used to execute the read display data mode. The display data byte is directly read from the GDDRAM. Please be noted that the $D/\overline{C}$ signal should be set to high during the display data is red from to the GDDRAM.

8.28 Register Status Read (F9 H)

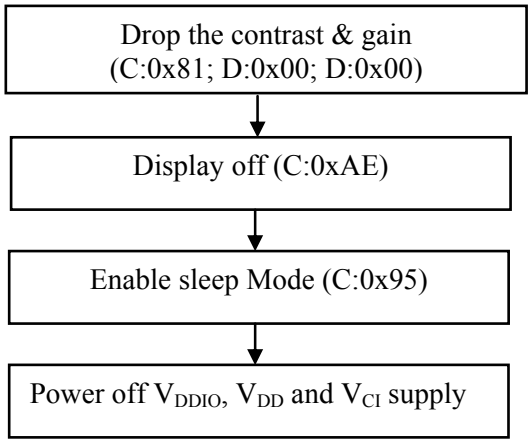
This command aims to read the register status. The OTP value and OTP register status can be read.

9 POWER ON/OFF SEQUENCE

Recommended Power On Sequence



Recommended Power Off Sequence



10 MAXIMUM RATINGS

Table 10-1: Maximum Ratings (Voltage Referenced to VSS)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{OUT}		-0.3 to 15	V
V_{CI}	Input Voltage	VSS-0.3 to 4.0	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC
Ron	Input Resistance	1000	ohm

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and Vout be constrained to the range VSS < VDDIO ≤ VDD ≤ VCI < VOUT. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Table 11-1: DC Characteristics (Unless otherwise specified, Voltage Referenced to VSS, $V_{DDIO}=V_{DD}=V_{CI}=2.775V$, $T_A=-40$ to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	System power supply pins of the logic block Range	Recommend Operating Voltage Possible Operating Voltage	2.4	2.7	3.3	V
V_{DDIO}	System power supply pins of logic block Range	Recommend Operating Voltage Possible Operating Voltage	1.7	-	V_{DD}	V
V_{CI}	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	V_{DD}	-	3.3	V
I_{AC}	Access Mode Supply Current Drain (V_{ci} Pins)	V_{CI} = 2.775V, Voltage Generator On, 6X DC-DC, Write accessing, Tcyc =5MHz, Frame Freq.= 35Hz, Display On, no panel attached.	-	450	550	µA
I_{DP}	Display Mode Supply Current Drain (V_{ci} Pins)	V_{CI} = 2.775V, V_{OUT} = 12V, Voltage Generator On, 6X DC-DC Converter Enabled, R/W(WR) Halt, Frame Freq.=35Hz, Display On, no panel attached.	150	260	450	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DDIO}, V_{DD} and V_{CI} Pins)	V_{CI} = 2.775V, LCD Driving Waveform Off, Oscillator Off, R/W(WR) halt. (25°C)	-	0.5	2	µA
$I_{StandBy}$	Stand By Mode Supply Current Drain (V_{DDIO}, V_{DD} and V_{CI} Pins)	V_{CI} = 2.775V, Oscillator On, LCD Driving Waveform Off	20	38	70	µA
V_{OUT}	LCD Driving Voltage Generator Output (V_{out} Pin)	Display On, Voltage Generator Enabled, DC-DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled.	-	-	15	V
	V_{OUT} Converter Efficiency	4X boost, no panel loading	-	99	99	%
		5X boost, no panel loading	-	96	99	
		6X boost, no panel loading	-	95	99	
		7X boost, no panel loading	-	92	98	
V_{OH1}	Logic High Output Voltage	Iout=-100uA	0.9*V_{DDIO}	-	V_{DDIO}	V
V_{OL1}	Logic Low Output Voltage	Iout=100uA	0.0	-	0.1*V_{DDIO}	V
V_{IH1}	Logic High Input voltage		0.8*V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Logic Low Input voltage		0.0	-	0.2*V_{DDIO}	V
I_{OH}	Logic High Output Current Source	Vout = V_{DD}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
ΔV_{OUT}	Variation of V_{OUT} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-	+/-2	-	%
TC0	Temperature Coefficient 0 (POR)	Voltage Regulator Enabled	-0.03	-0.01	0.00	%/°C
TC1	Temperature Coefficient 1		-0.07	-0.06	-0.05	%/°C

The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{out}at50°C - V_{out}at0°C}{50°C - 0°C} x \frac{1}{V_{out}at25°C} x100\%$$

12 AC CHARACTERISTICS

Table 12-1: AC Characteristics
(Unless otherwise specified, Voltage Referenced to V_{SS}, $V_{DDIO}=V_{DD}=V_{CI}=2.775V$, $T_A = 25°C$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{FRM}	Frame Frequency for: 130 x 130 MUX Mode	V_{CI}=2.775V, Display ON, Internal Oscillator Enabled	-	56.4	90	Hz

Table 12-2: Parallel 6800-series Interface Timing Characteristics
(T_A = -40 to 85°C, V_{DDIO}=2.775V, 2.775V≤V_{DD}≤V_{CI}≤3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	-	100	-	ns
PW_{CSL}	Control Pulse Low Width	-	50	-	ns
PW_{CSH}	Control Pulse High Width	-	50	-	ns
t_F	Fall Time	-	-	10	ns
t_R	Rise Time	-	-	10	ns
t_{AS}	Address Setup Time	-	10	-	ns
t_{AH}	Address Hold Time	-	10	-	ns
t_{DSW}	Data Setup Time	-	60	-	ns
t_{DHW}	Data Hold Time	-	25	-	ns
t_{ACC}	Data Access Time	-	275	-	ns
t_{OH}	Output Hold time	-	125	-	ns

Figure 12-1: Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

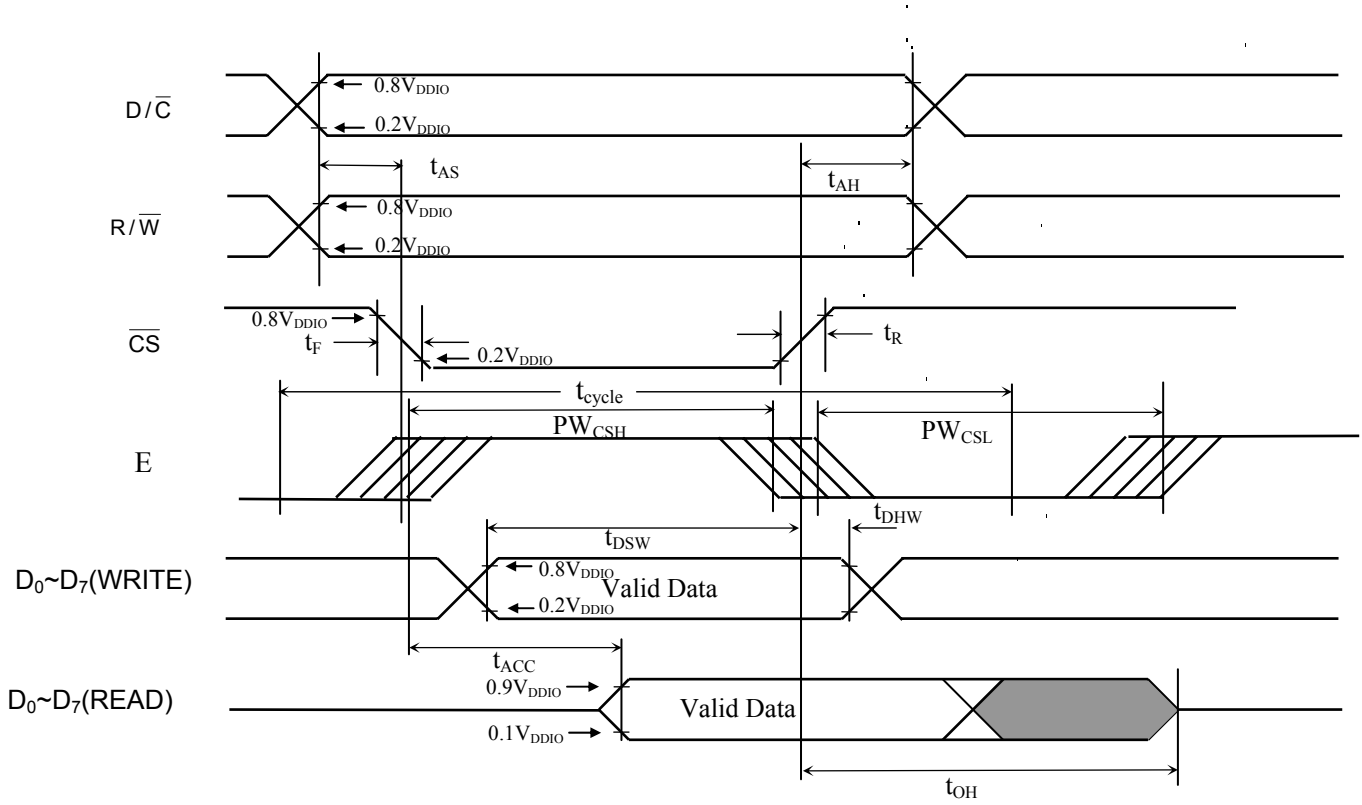


Table 12-3: Parallel 8080-series Interface Timing Characteristics
(T_A = -40 to 85°C, V_{DDIO}=2.775V, 2.775V≤V_{DD}≤V_{CI}≤3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	-	100	-	ns
PW_{CSL}	Control Pulse Low Width	-	50	-	ns
PW_{CSH}	Control Pulse High Width	-	50	-	ns
t_F	Fall Time	-	-	10	ns
t_R	Rise Time	-	-	10	ns
t_{AS}	Address Setup Time	-	10	-	ns
t_{AH}	Address Hold Time	-	10	-	ns
t_{DSW}	Data Setup Time	-	60	-	ns
t_{DHW}	Data Hold Time	-	25	-	ns
t_{ACC}	Data Access Time	-	275	-	ns
t_{OH}	Output Hold time	-	125	-	ns

Figure 12-2: Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

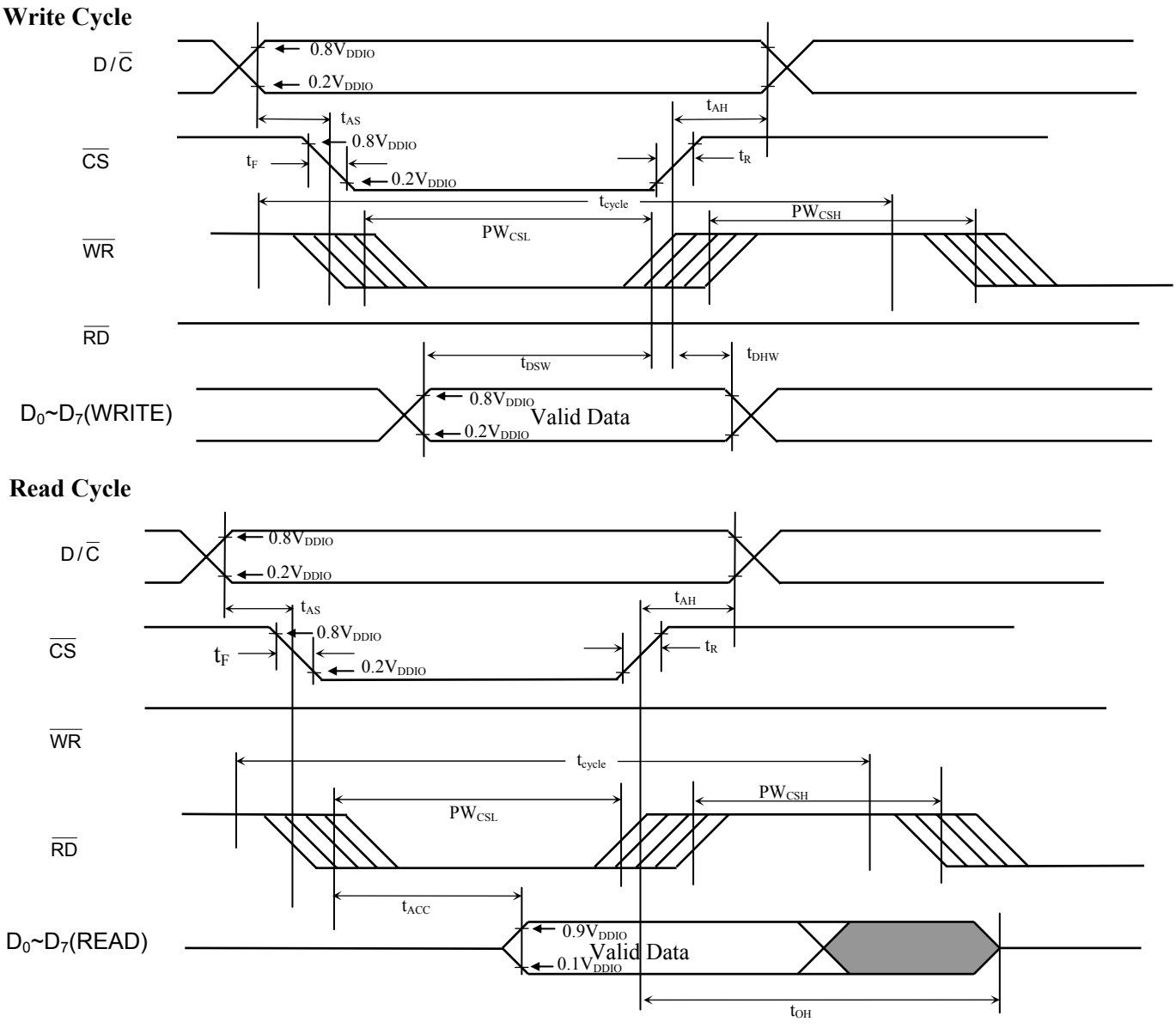


Table 12-4: 4-Wires Serial Timing Characteristics
(T_A = -40 to 85°C, V_{DDIO}=2.775V, 2.775V≤V_{DD}≤V_{CI}≤3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	-	100	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	10	-	MHz
t_{AS}	Register select Setup Time	20	-	-	ns
t_{AH}	Register select Hold Time	30	-	-	ns
t_{CSS}	Chip Select Setup Time	-	35	-	ns
t_{CSH}	Chip Select Hold Time	-	50	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_F	Fall Time	-	-	10	ns
t_R	Rise Time	-	-	10	ns
t_{CLKL}	Clock Low Time	-	50	-	ns
t_{CLKH}	Clock High Time	-	50	-	ns

Figure 12-3: 4-Wires Serial Timing Characteristics (PS0 = L, PS1 = H)

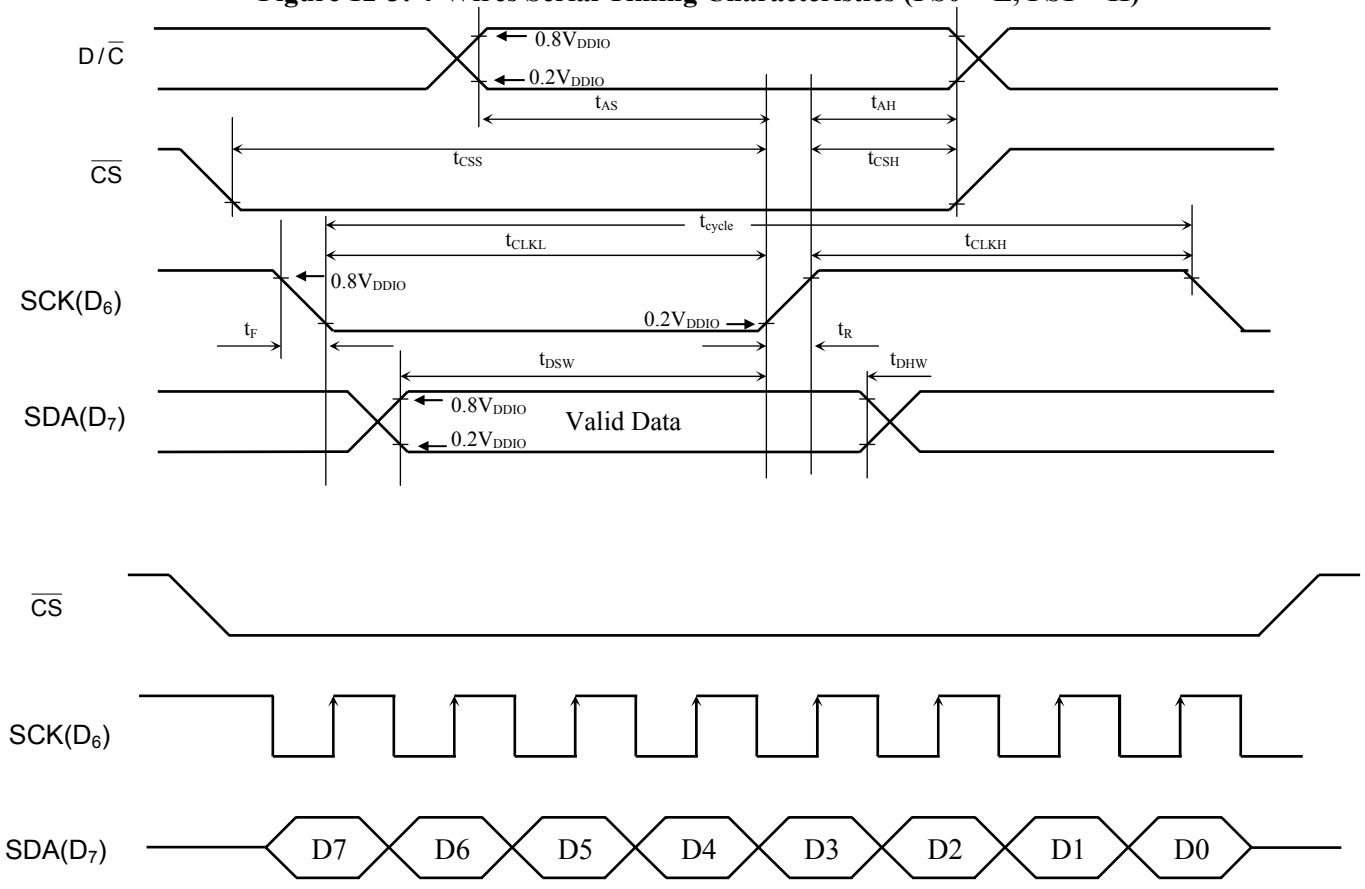
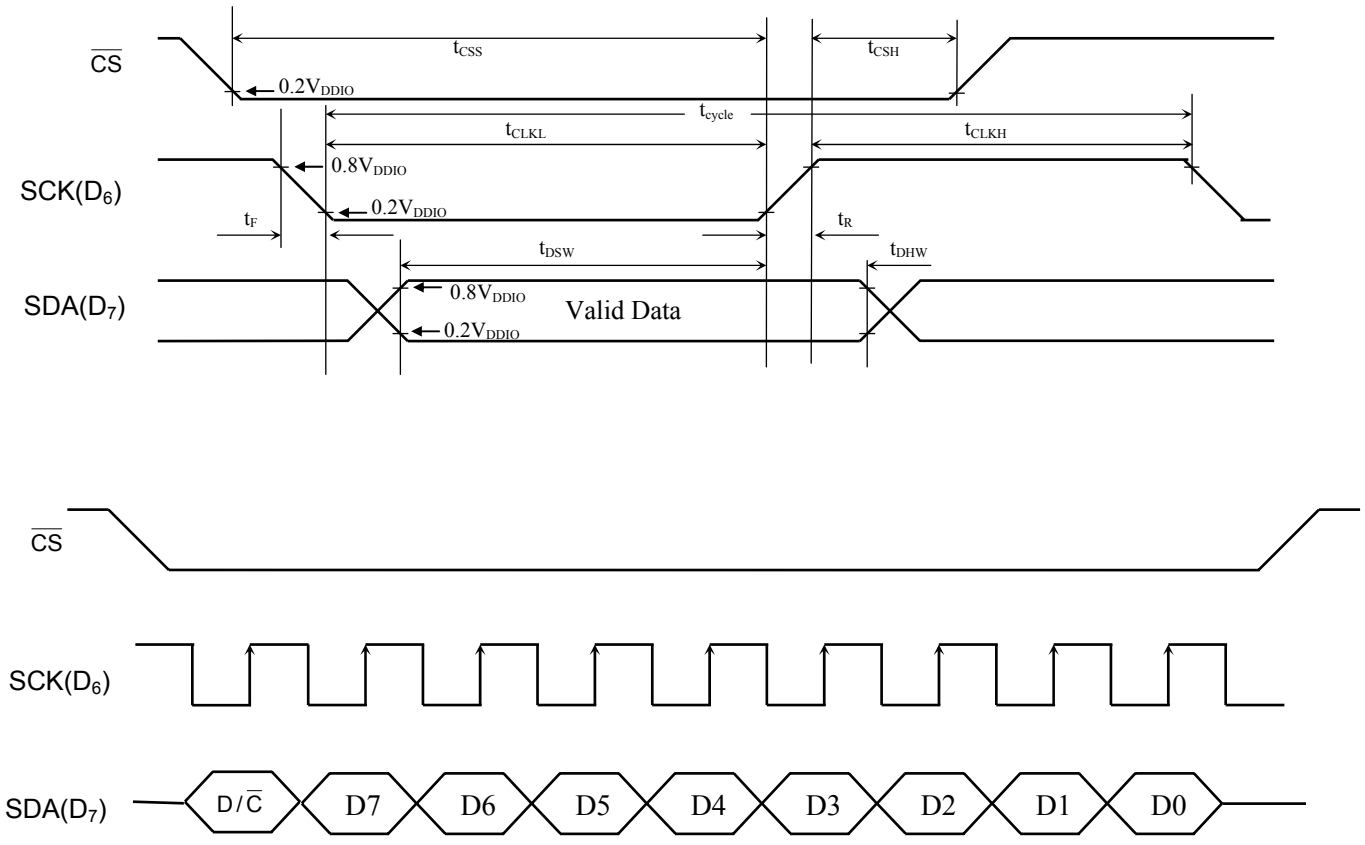


Table 12-5: 3-Wires Serial Timing Characteristics
(T_A = -40 to 85°C, V_{DDIO}=2.775V, 2.775V≤V_{DD}≤V_{CI}≤3.3V)

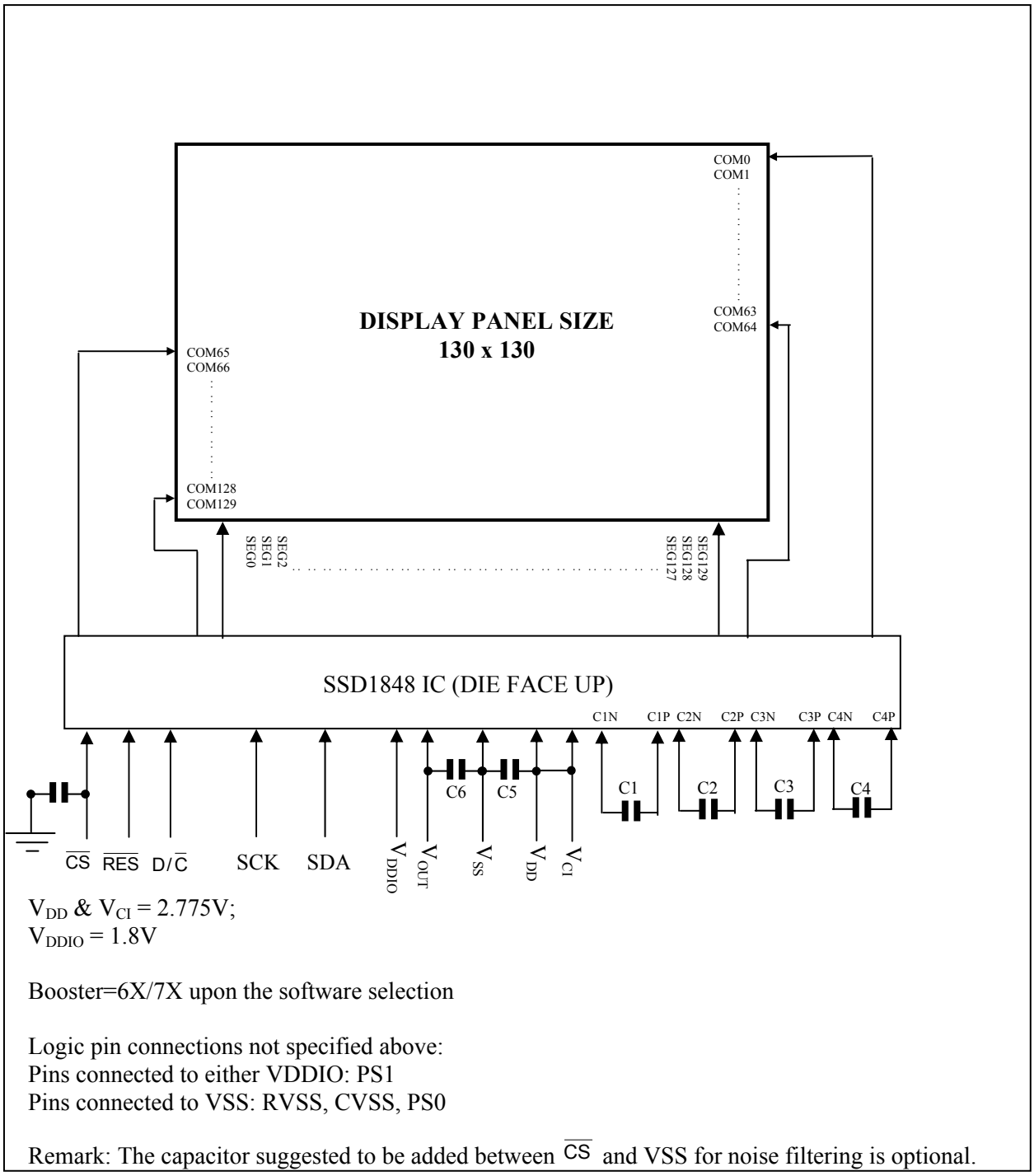
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	-	100	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	10	-	MHz
t_{CSS}	Chip Select Setup Time	-	35	-	ns
t_{CSH}	Chip Select Hold Time	-	50	-	ns
t_{DSW}	Write Data Setup Time	-	35	-	ns
t_{OHW}	Write Data Hold Time	-	50	-	ns
t_F	Fall Time	-	-	10	ns
t_R	Rise Time	-	-	10	ns
t_{CLKL}	Clock Low Time	-	50	-	ns
t_{CLKH}	Clock High Time	-	50	-	ns

Figure 12-4: 3-Wires Serial Timing Characteristics (PS0 = L, PS1 =L)



13 Application Diagram

Figure 13-1: Application Examples I (4-wires SPI mode)



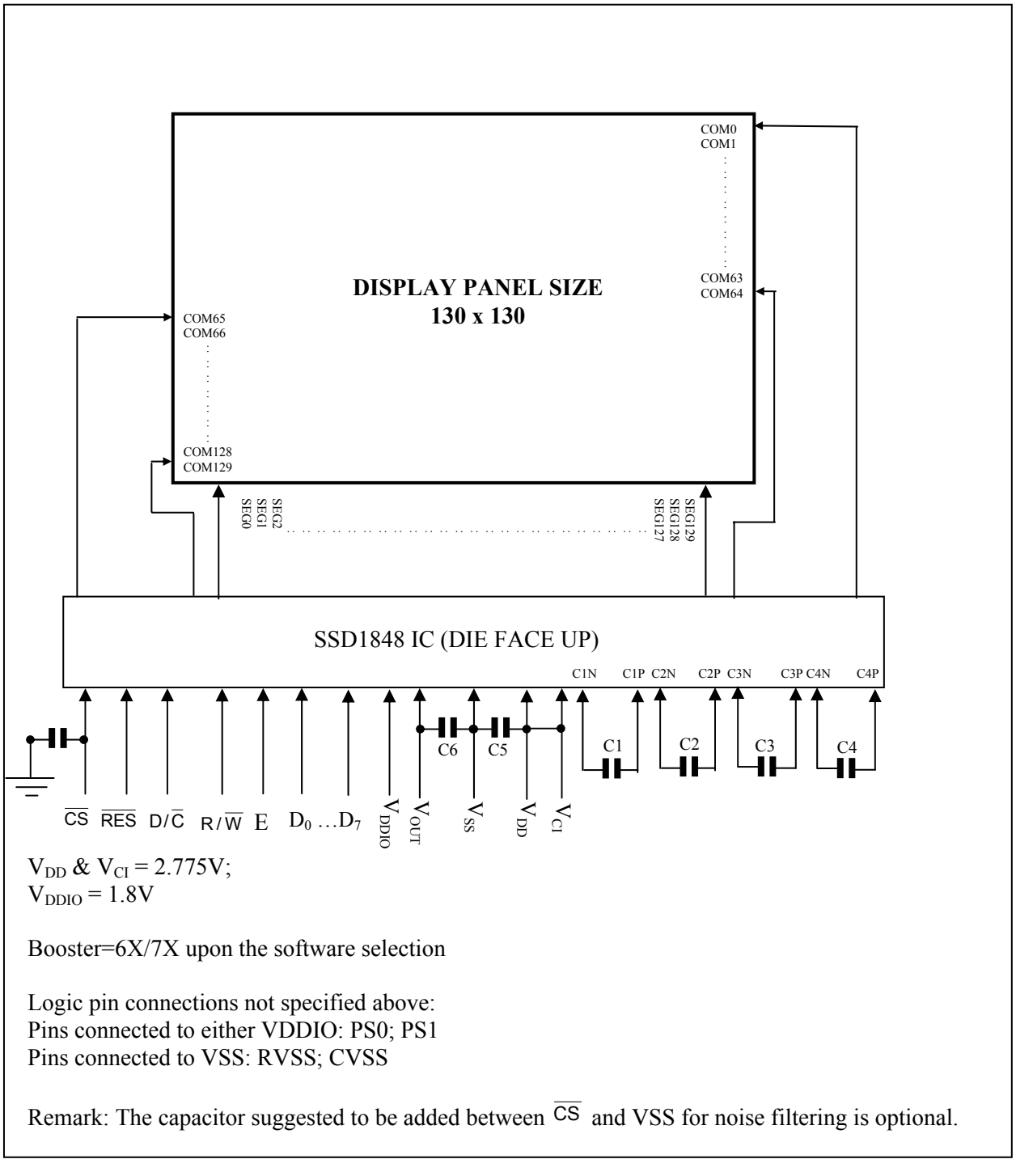
V_{DD} & V_{CI} = 2.775V;
V_{DDIO} = 1.8V

Booster=6X/7X upon the software selection

Logic pin connections not specified above:
Pins connected to either VDDIO: PS1
Pins connected to VSS: RVSS, CVSS, PS0

Remark: The capacitor suggested to be added between $\overline{CS}$ and VSS for noise filtering is optional.

Figure 13-2: Application Examples II (6800 PPI mode)



V_{DD} & V_{CI} = 2.775V;
V_{DDIO} = 1.8V

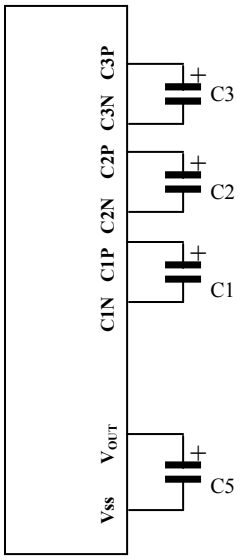
Booster=6X/7X upon the software selection

Logic pin connections not specified above:
Pins connected to either VDDIO: PS0; PS1
Pins connected to VSS: RVSS; CVSS

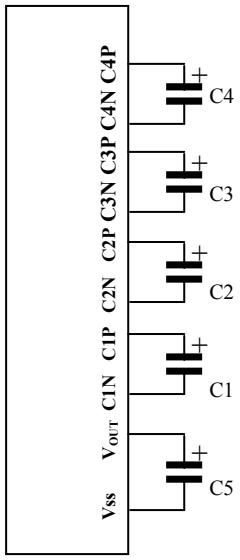
Remark: The capacitor suggested to be added between $\overline{CS}$ and VSS for noise filtering is optional.

Figure 13-3: Booster configuration

4X/5Xbooster



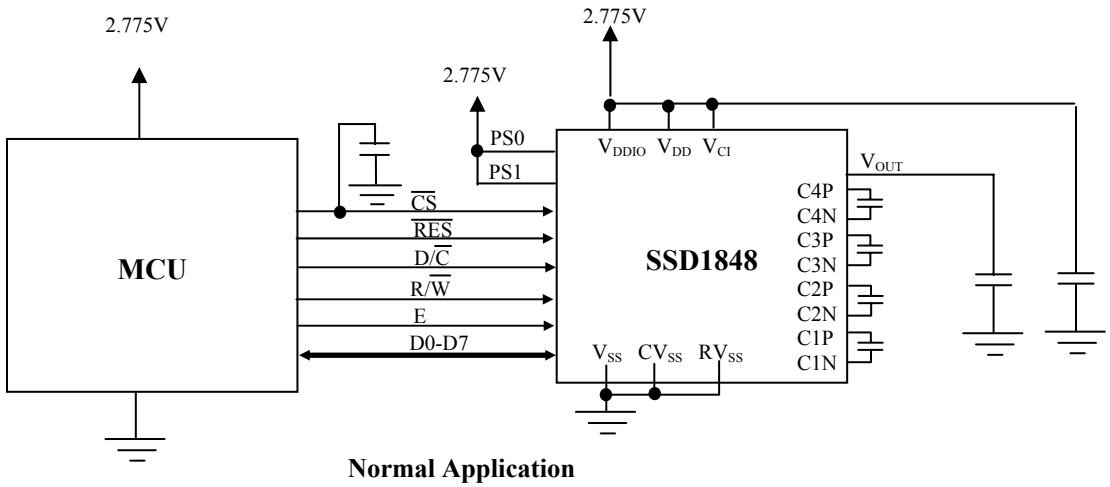
6X/7X booster



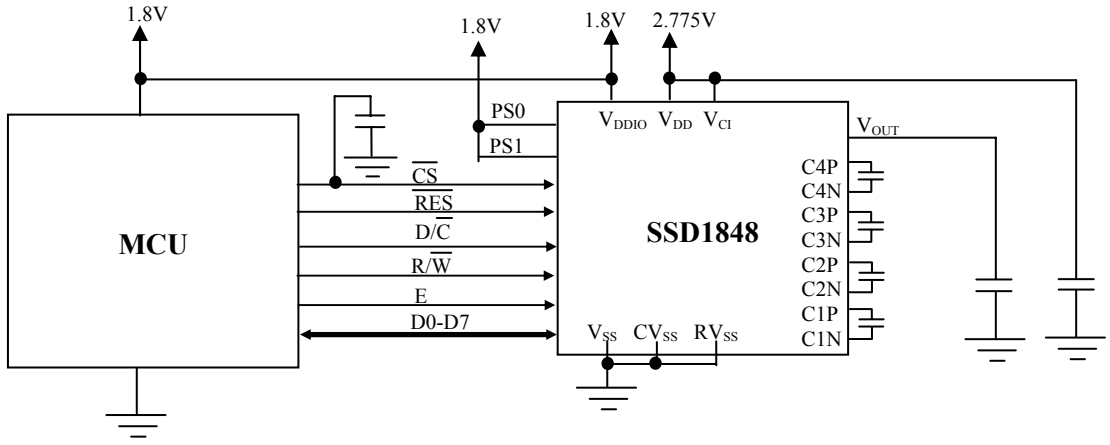
Note:
C1, C2, C3 and C4 ≥ 0.1µF
C5 ≥ 1µF
C5 ≥ C1, C2, C3 and C4

Voltage rating:
C1: 1 x VCI
C2: 2 x VCI
C3: 3 x VCI
C4: 5 x VCI
C5: 25V

Figure 13-4: Applications notes for VDD/VDDIO connection



Normal Application

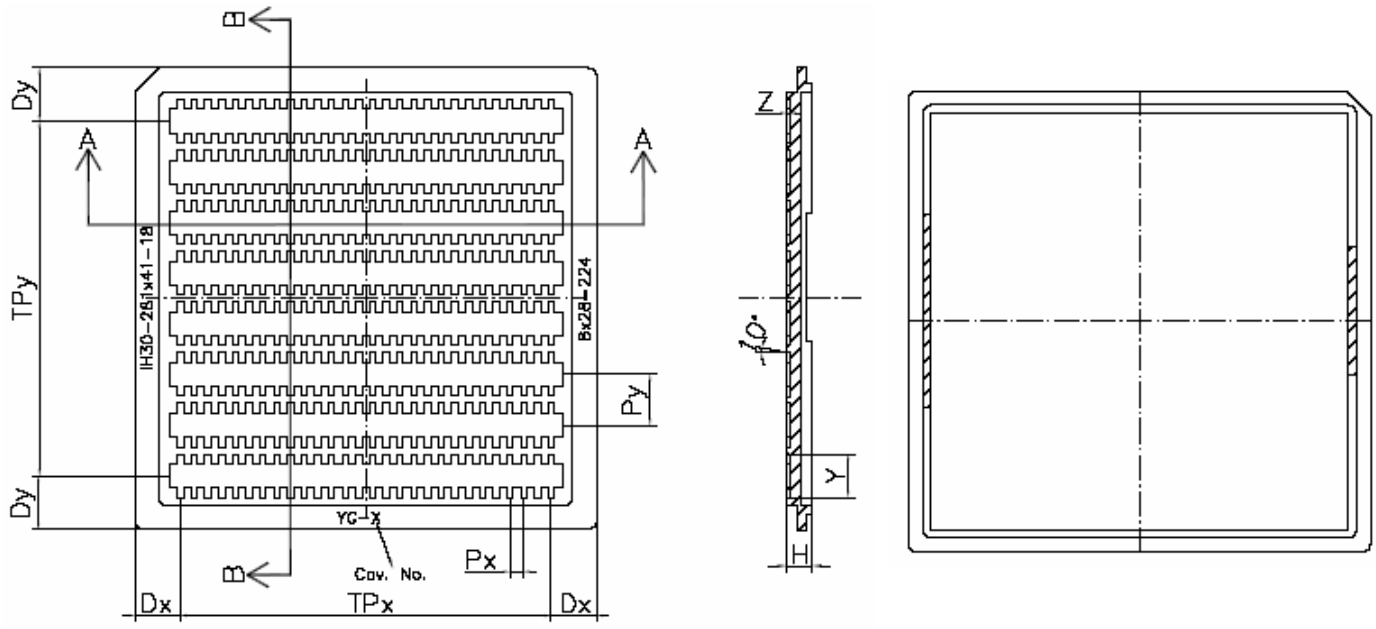


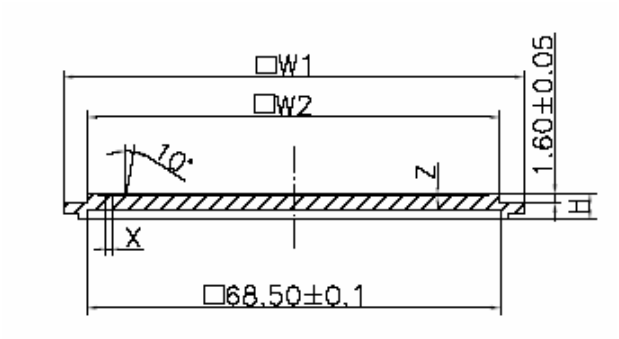
Low Voltage MCU

Remark: The capacitor suggested to be added between $\overline{CS}$ and VSS for noise filtering is optional.

14 PACKAGE INFORMATION

14.1 DIE TRAY DIMENSIONS



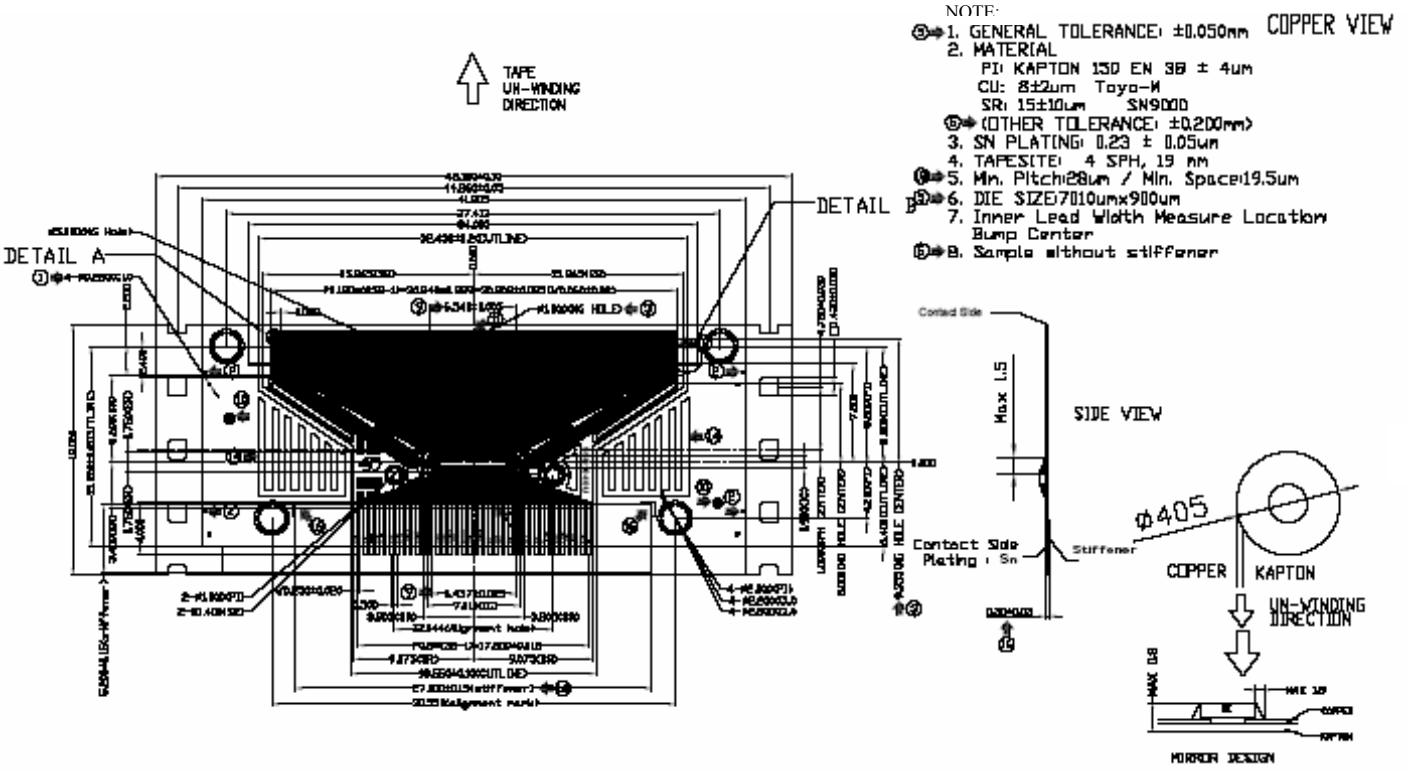


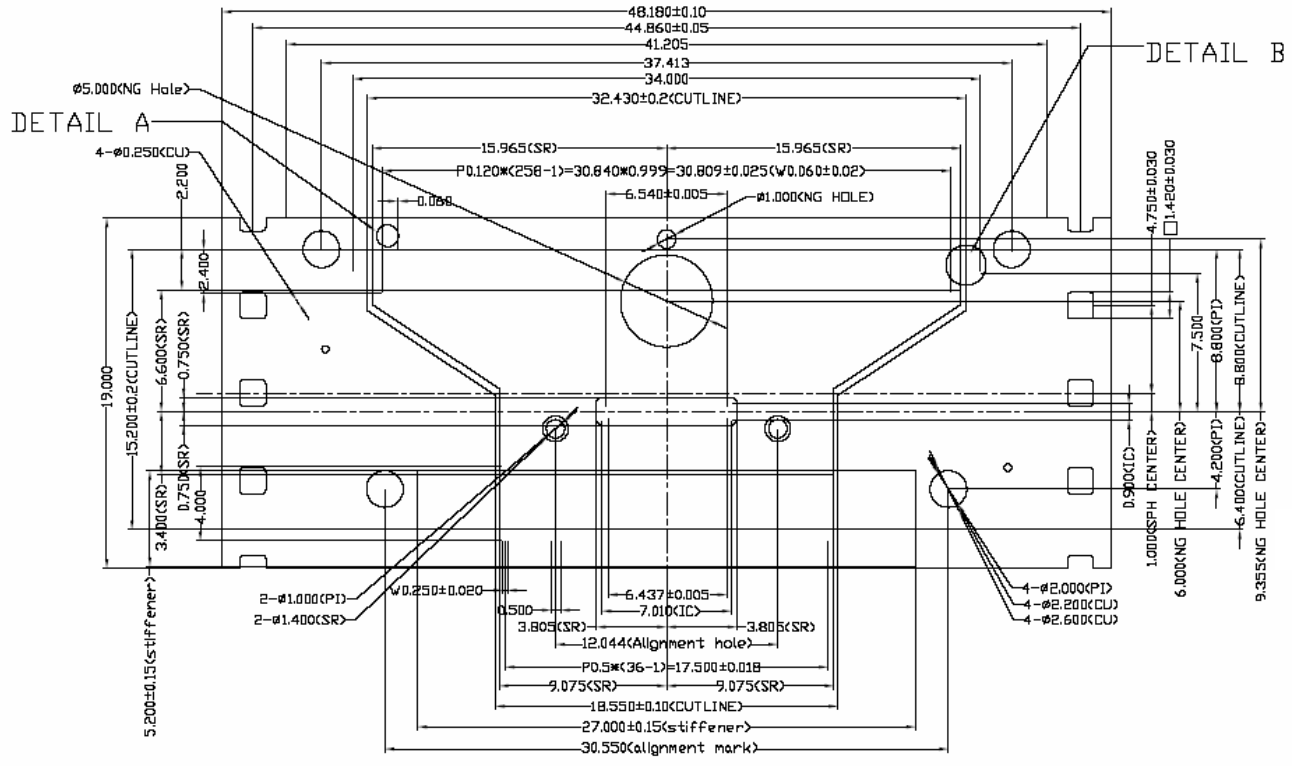
Spec	mm	(mil)
W1	76.00 +/- 0.10	2992
W2	68.00 +/- 0.10	2677
H	4.20 +/- 0.10	165
Dx	7.49 +/- 0.10	295
TPx	61.02 +/- 0.10	2402
Dy	8.84 +/- 0.10	348
TPy	58.31 +/- 0.10	2296
Px	2.26 +/- 0.05	89
Py	8.33 +/- 0.05	328
X	1.03 +/- 0.05	41
Y	7.14 +/- 0.05	281
Z	0.46 +/- 0.05	18
N	224 (pocket number)	

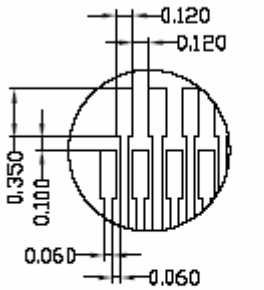
NOTE:

1. THE BOTTOM OF POCKET: ROUGH SURFACE
2. TRAY COLOR: BLACK

15 SSD1848U COF DRAWING

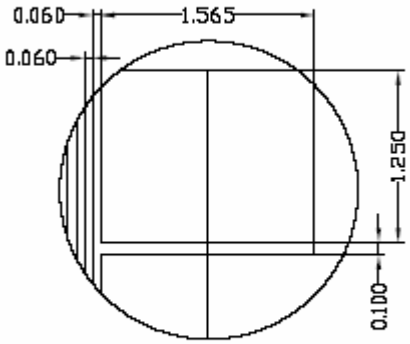






DETAIL A

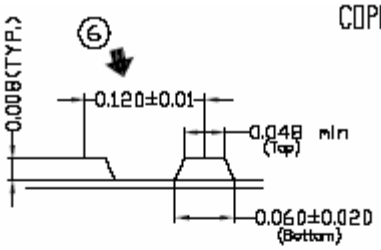
⑧➡SCALE 5:1



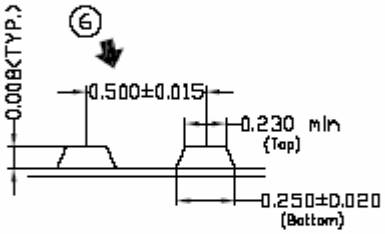
DETAIL B

⑧➡SCALE 5:1

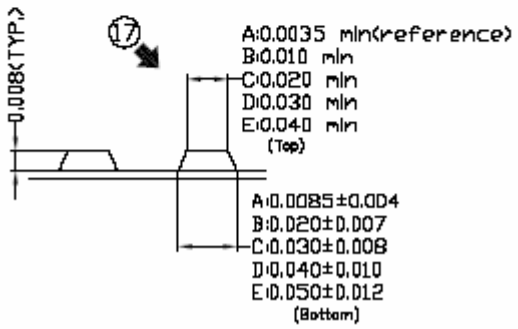
COPPER VIEW



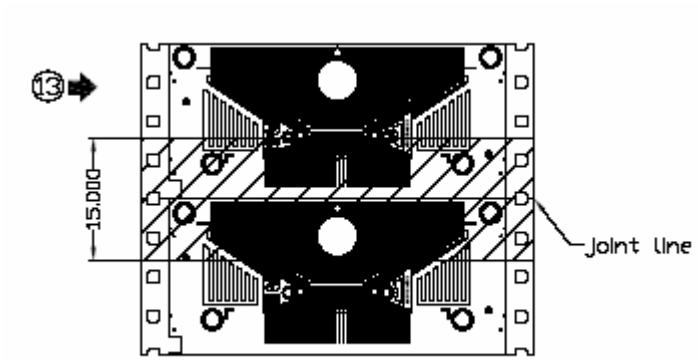
OUTPUT SIDE OUTER LEAD CROSS SECTION



INPUT SIDE OUTER LEAD CROSS SECTION



INNER LEAD CROSS SECTION



All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) “Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)” and China standard “电子信息产品污染控制标识要求 (SJ/T11364-2006)” with control Marking Symbol . Hazardous Substances test report is available upon requested.

http://www.solomon-systech.com